

**POWER ELECTRONICS BUILDING BLOCKS
AND SYSTEM INTEGRATION**

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Chapter 1 Executive Summary

1.1 Advanced Power Semiconductor Devices

In this part of the research work, both two-terminal high-voltage rectifiers and three-terminal MOS-gated power transistors have been studied. We have designed a mask set for the 3000V TSOX-MPS rectifier based on the numerical analysis of the forward, reverse, and switching characteristics. The 3000V TSOX-MPS rectifiers are presently in the process of being fabricated, and should be completed within the next four months. We will characterize for functional yield, provide the die for packaging and system-level evaluation, and calibrate them based on simulated results. The first lot of IGBTs and IGBT/BRTs has been completed with decent performance and yield. More destructive tests are needed for the IGBTs and IGBT/BRTs to verify the latch-up current and SOA have been conducted. The successful fabrication of the MOS-gated bipolar devices in the microelectronics clean room in the Rensselaer Polytechnic Institute shows the semiconductor device fabrication capability of the advanced power device research group in RPI.

1.2 Active IGBT Gate Driver and High Performance Drive

The research work on the active gate drive has been carried out. The current effort has mainly focused on issues of integrating the three-stage active gate drive with fast fault current limiting protection circuits for high-power IGBT PEBBs to improve the overall reliability of the power converter. The temperature rise of the switch module and its effects on the three-stage active gate drive strategy has been studied in detail. The active gate drive performance have been tested with both PT and NPT IGBTs. Efforts to characterize the three-stage active gate drive with HVIGBTs available from various manufacturers are proceeding. Test results have been obtained from the integrated three-stage active turn-on and turn-off gate driver with a fast fault current limiting protection circuit. The proposed three-stage active gate drive technique's ability to operate under the wide range of temperature conditions experienced by the devices has been verified. The integrated fast fault protection circuit allows the active gate drive to operate at a higher

on-state gate voltage, which leads to reduction of the conduction loss. Also, due to the fault management strategy, the active drive circuit can considerably improve the fault endurance capability of the device. The state transition description for the three-stage active gate drive with the protection circuit, the testing hardware setup description, the experimental switching transient waveforms, the quantitative data and the discussion of the effect of temperature and short circuit protection test results have all been presented. Through this work, it has been verified that the three-stage active gate drive adapts itself to a wide range of operating conditions with the fast fault current limiting technique. Such characteristics are especially important for the high voltage IGBTs that are available today and for standardization of high-power IGBT switches in the form of a power electronics building block.

The second aspect of this research work involves the control strategies for a hybrid seven-level inverter. This work is devoted to the investigation of control techniques applicable for a seven-level hybrid inverter. In particular, analysis of a hybrid modulation technique, which incorporates stepped synthesis in conjunction with the variable pulse width of the consecutive steps, has been performed. Additionally, variations of multi-carrier pulse width modulation (PWM) techniques related to the disposition and phase shifting and their comparative evaluation have been performed. The performance attributes of conventional techniques such as staircase modulation and programmed PWM have been assessed and the optimization of switching angles to minimize the harmonic distortion at different modulation depth has been analyzed. Operating principles, spectral structure, and other practical issues, e.g. power interaction between two H-bridge power converters, have been studied. The preliminary simulation results from Matlab/Simulink and the representative experimental waveforms have been obtained during the research. These studies are foundation of the more detailed and practical simulation model and the hardware implementation and its performance verification.

The third aspect of this research work involves the simulation of the hybrid multilevel inverter system. A detailed simulation model for the seven-level hybrid inverter with *Saber* has been built. The model description includes transformers for isolation and

voltage matching, a rectifier front-end, a hybrid seven-level inverter (an IGCT inverter and an IGBT inverter), and a modulation signal generating scheme. The rectifier front-end and inverter front-end blocks are dealt with as hybrid cells. Steady-state simulation results for various values of modulation depth and typical transient charging process simulation results are presented. The hybrid inverter output voltage and current spectra have been examined, and the preliminary study results verify the control strategies for the inverter.

The last research effort involves the hardware prototyping of the hybrid multilevel inverter, including a DSP-based controller. The system is supplied from a net DC voltage bus of 3300 Volts and split in the ratio 2:1, where the corresponding two H-bridge modules are built using integrated gate commutated thyristors (IGCT) and an IGBT. The hardware consists of a power stage, controller, and fault detection/protection parts. The DC bus charge-up test data, and individual and hybrid inverter test data are all presented in the experimental results. The results obtained from the same operating condition as in the circuit simulation with *Saber* correlate well with the simulation results, therefore verifying the validity of the modulation scheme. Henceforth, the feasibility of hybrid multilevel inverter system as a well-modularized medium-voltage power converter system for Power Electronics Building Blocks has been experimentally demonstrated.

1.3 Testbed for System Integration

The soft-switched DC bus regulator has been successfully tested under high power levels with a 20kHz switching frequency and a 40kHz sampling frequency. Both of the current and voltage feedback loops are closed. The maximum power level for the power stage is tested up to 70kW. Major associated issues have been solved in the tests. Therefore, this soft-switched DC bus regulator is ready for system integration. A DSP control program has been developed for the butterfly valve. Therefore, this DC bus regulator can also be configured as a motor drive inverter in a PNP demonstration system.

Several issues are explored in the tests. One issue is the problem of low-frequency harmonics caused by the PWM. Three causes have been identified: pulse width limits; a space vector modulation (SVM) scheme; and dead time. Another issue is the problem of

thermal and electrical stress in the resonant capacitor for the soft switching. This issue is basically solved by the modulation techniques in the three-phase operation.

The research on the four-leg secondary utility power supply has been carried out. A four-leg inverter system has been implemented to provide a four-wire three-phase system to control the zero sequence component of the load current for unbalanced/nonlinear loads. As part of the PEBB DC DPS testbed, stand-alone tests of the hardware setup have been conducted intensively with different kind of loads, including balanced/unbalanced, linear/nonlinear cases.

Besides the above-mentioned tests, some issues relating to different 3-D SVM schemes have been explored. One issue is over-modulation in the 3-D SVM. With the space geometrical analysis, the 3-D SVM over-modulation boundary is then defined. Two over-modulation correction schemes have been proposed and implemented to confine the SVM operation within necessary boundaries. The proposed over-modulation schemes, along with the system without over-modulation correction, are compared with time-domain simulation and harmonic frequency analysis. With the proposed Scheme 1, the output voltage waveform quality can be improved, but distortion can be severe under unbalanced load conditions. With the proposed Scheme 2, which confines the voltage vector to an inner surface, the voltage distortion can be nearly eliminated. However, its available magnitude is reduced. Another issue is the presence of common-mode EMI in three-dimensional space vector modulation. Nine 3-D SVM schemes were investigated from the EMI point of view. The trade-off research has been done on the selection of SVM schemes. Of the nine schemes, an optimal scheme has been found, which is the symmetrically aligned Class II scheme (SVM2).

When the secondary utility bus subsystem is integrated into the system, it will present two challenges to the DC bus. With the possibility of unstable DC bus voltage due to unbalanced and nonlinear load effects, a 30 kW bus conditioner has been proposed, implemented, and tested in this research. When the load of the subsystem is unbalanced, the subsystem behaves like a nonlinear load to the DC bus. A great amount of ripple current has to be absorbed by the DC bus. The ripple current represents a large signal

perturbation to the DC bus. However, the voltage control loop for the front-end boost rectifier(s) is designed based on the assumption that there will be small signal perturbation on the DC bus. The DC bus may run into instability in this case. An even worse condition is when there are several unbalanced three-phase subsystems. In this case, those ripple currents with difference frequencies and phases will interact with each other. This would be a far more severe situation for the DC bus than the first situation described. In this project, the nonlinear loading effect to the DC bus is characterized first. The proposed bus conditioner is then implemented and tested. The switching frequency has been pushed up to 50 kHz.

The DC bus conditioner is a novel concept for the DC distributed power system. A bi-directional DC/DC converter is used for the bus conditioner, which shunts the large signal AC current, which is otherwise on the DC bus, into an isolated energy storage component so that the DC bus and source converter are free from its contamination. The DC bus conditioner decouples the AC dynamic load from the DC bus. It also improves the transient performance of the DC bus, actively shapes the input impedance of the regulated converter or the output impedance of the source converter, and provides more stability margins to distribution systems. The DC bus conditioner has been constructed and preliminary tests have been carried out.

For a high-power DPS system, the parallel operation of several converters is inevitable. It is natural to parallel standardized PEBB modules in PEBB systems. However, potential interactions, such as small-signal interaction and zero-sequence interaction, may occur. To avoid the potential interactions, traditionally a parallel converter system either has a transformer on the AC side or uses separate power supplies. In these cases, the parallel converters are not coupled and can be designed individually. One major disadvantage of this solution is that the overall parallel system is bulky and expensive because of the line-frequency transformer and the additional power supplies. With more converters in parallel, this solution practically becomes unaffordable.

In order to reduce size and cost, a directly connected parallel converter structure is desirable. The non-isolated (also called transformerless) parallel connection of converters

presents attractive characteristics such as simplicity, easy expandability, easy maintainability, high availability, possibly de-rated operations with failed elements, and suitability for low-voltage high-current applications, such as in superconductors.

Even with all these advantages, the risk would be high. Few systems with parallel non-isolated multi-phase converters are put into practice because of the coupling dynamics and the potential interactions between the parallel converters.

Usually, the control design for a single converter does not take care of zero-sequence components because there is no zero-sequence current path. This path, however, is formed in the parallel non-isolated converters. In this work, an averaged model predicting the dynamics of the zero-sequence current is developed using a phase-leg averaging technique. Based on the model, this work proposes a new control scheme to suppress the zero-sequence current. Since the new control scheme is designed within the individual converter and does not need any additional interconnected circuitry, it allows modular design.

This modeling and control concept is then generalized to any parallel multi-phase converters, such as full-bridge rectifiers and inverters, three-phase, three-leg rectifiers and inverters, and three-phase, four-leg rectifiers and inverters. These converters cover most medium- and high-power applications.

Because of their symmetrical structure, parallel converters offer an opportunity to reduce the high-frequency common-mode dv/dt noise. After examining the nature of the common-mode dv/dt noise, this work proposes a new modulation strategy for a synchronized two-parallel non-isolated multi-phase converter system to reduce the common-mode noise. Since the new modulation is essentially an interleaving scheme, the differential-mode ripple is also reduced.

“Plug and play” has become a major focus in the PEBB research. We have put tremendous effort into this research work, including taking part in the PCIM show in Chicago, organized by the ONR.

In medium- and high-power converters, which have spatially distributed hardware, spatially distributed sensors (meaning that system data are distributed) and which require different levels of control, the need for new, advanced distributed control architecture that will reduce development time, increase reliability, and allow for simple reconfiguration and maintenance is needed.

Proposed and designed control architecture consists of smart power modules, universal DSP controllers, and smart sensors all linked into a coherent control structure by means of an open and flexible fiber-optic communication link. All these elements make the whole system flexible, multi-functional, and easy to use. Using newly designed smart modules, new universal DSP controllers, and new smart sensors, the three-phase 100 kW inverter has been designed and tested to show the concept and further explore the potential of this approach.

The main benefits of this approach can be summarized as follows:

- Open control architecture
- Reduced converter wiring
- Highly modular design
- Simple reconfiguration
- Reduced power converter design cycle
- System oriented thinking

Not only does this approach allow us to easily reconfigure and adapt the system or part of the system but it also shows the promise of bringing down the cost of power electronics systems in both development and production. Furthermore, it paves the way toward the "plug and play" approach in power electronics, which would allow the shift toward system-oriented design and thinking from circuit-oriented design.

Integration, modularization, and object-oriented approaches, which revolutionized areas such as computers and communications, are slowly penetrating power electronics. Therefore, we believe that our approach is providing the necessary tools and ideas for a future revolution in power electronics design and thinking.

Besides all the effort and achievement mentioned above, we also started a research work on what we consider a viable technology in the future – a matrix converter (MC). In a matrix converter, each output phase can be directly connected to any input phase within any long period at any time. So, among all kinds of power conversions MC has the highest flexibility controlling both output and input waveforms. This means that MC has some excellent characteristics, such as: the ability to convert from any frequency to any frequency; sinusoidal waveforms on both output and input sides; unity or displaceable input power factor.

Besides these, the MC has lots of other positive characteristics.

The research work we have started includes the preliminary design of a 15 kVA and its hardware and software implementation. The power stage topology and control scheme will be tested and verified during the next phase.

Chapter 2 Advanced Semiconductor Devices

2.1 INTRODUCTION

Semiconductor power devices form the fundamental building blocks of any power electronics circuits and systems. One of the thrust areas on which ONR PEBB research program is focused on is the development of advanced novel power semiconductor devices that are not currently commercially available.

The objective of the power semiconductor thrust area is to explore, develop and demonstrate advanced power semiconductor devices with improved performance than state-of-the-art commercially available power devices such as the insulated gate bipolar transistor (IGBT) and mos-controlled thyristor (MCT). During the past year, several new power semiconductor devices other than the IGBT and MCT have been proposed. They include the emitter switched thyristor (EST), base resistance controlled thyristor (BRT), dual gate BRT (DG-BRT) and merged IGBT-BRT and IGBT-MCT structures.

2.2 GENERAL OVERVIEW OF NOVEL DEVICES

2.2.1 TSOX-MPS RECTIFIER

The recent trend of power electronics systems can be summarized as having decreasing size and increasing efficiency. This has been achieved by high-frequency operation. High-frequency operation in power electronics systems requires high speed switching semiconducting components such as transistors and diodes. The *p-i-n* rectifier, well known as conducting high forward current and high reverse blocking voltage, has been used widely in high voltage applications despite its slow switching speed. On the other hand, the Schottky rectifier usually preferred for lower voltage ratings (<100V) exhibits fast switching because of its unipolar nature as far as switching high voltage at high frequency.

Fast switching with reasonably low forward drop of the rectifier was achieved by merging the *p-i-n* rectifier and with the Schottky rectifier [1][2]. In the MPS rectifier, the

Schottky and the p - n junctions are merged in a single body as an anode. The p^+ junctions are diffused in the Schottky junction to enhance the blocking voltage. The MPS rectifier, however, shows high reverse leakage current compared to that of the p - i - n rectifier.

It has been claimed that the TSOX MPS rectifier shows a low reverse leakage current (as small as that of the p - i - n rectifier) while switching several times faster than the p - i - n rectifier. The structure of the TSOX MPS rectifier is shown in Figure 2-1. In this structure, minority carriers are injected into the lightly doped drift region when the anode-to-cathode voltage exceeds a junction drop, typically 0.7V to reduce the voltage drop in the drift region while the majority carriers are flowing through the Schottky contact. When a reverse-bias voltage is applied to this device, depletion regions between the p^+ and n^- regions are merged in the mesa regions so that the potential at the Schottky junction remains at low-voltage and high reverse voltage is supported across this depletion region. This allows the device to support voltage as high as the p - i - n rectifier. Furthermore, the switching speed is also fast because the charges stored in drift layer are less than those of the p - i - n rectifier. Additionally, the MOS region minimizes the reverse leakage current in the reverse blocking state compared with that of a merged p - i - n /Schottky rectifier.

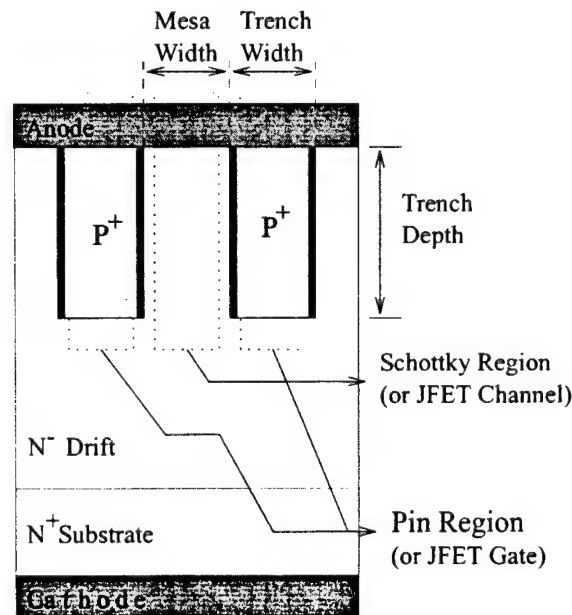


Figure 2-1. Cross-sectional view of TSOX MPS rectifier.

2.2.2 IGBTD

The IGBT is one of the most popular devices in power electronics. Its gate control coupled with a wide safe operating area (SOA) makes the IGBT the device of choice for many power converter applications. In an attempt to improve upon the IGBT, the IGBT with diverter (IGBTD) was conceived. By adding a diverter terminal shorted to the emitter, an alternate path for the hole current to be collected was formed. This reduces the hole current flow through the P-base region compared to the conventional IGBT. The result is improved latching current density, which leads to an increase of the forward-biased SOA (FBSOA)[4]. In this project, RPI has designed the IGBTD to have a current rating of 0.25A and the voltage rating of 600V. The fabrication was done at RPI's class 100 clean room. The fabricated devices were characterized for both static and dynamic parameters and compared with the baseline IGBT, which was fabricated in the same lot.

2.2.3 IGBT/BRT

In recent years, MOS-gated bipolar devices have gained increasing popularity because of their low forward voltage drop and simplicity of drive circuit resulting from their high input impedance. Among these devices, the IGBT has emerged as the most popular commercially available device as it is able to conduct current with low forward voltage drop because of the conductivity modulation of its low-doped base region. Its structure has been optimized to improve the trade-off curve between on-state voltage drop (V_f) and turn-off time (t_f) to minimize power losses in applications. In addition to this trade-off, it has been found that a good FBSOA and a good reverse biased safe operating area (RBSOA) are essential for controlling the rate of current changing during device turn-on/turn-off and for short-circuit protection. Consequently, it has been found that the optimization of the IGBT structure must be performed with three device parameters: namely, V_f , t_f and SOA. A superior trade-off curve between V_f and t_f can be achieved in MOS-gated thyristor structures when compared with the IGBT. Among these devices, the MCT [6] and BRT [7] have the lowest V_f , similar to that of a thyristor. However, they do not exhibit current saturation capability and therefore lack FBSOA. The EST [8] has a good FBSOA, but its V_f is 0.5 to 1V larger than that of the thyristor resulting in an inferior V_f - t_f trade-off curve when compared with the MCT or BRT. A dual-gate MOS

thyristor (DGMOS) structure [9], containing two lateral N-channel MOSFETs with separate thyristor and IGBT regions, has been previously proposed. It was demonstrated by numerical simulation that current flow could be switched between the thyristor region and the IGBT region.

In order to get a good trade-off curve between forward voltage drop and turn-off time while maintaining an improved FBSOA, we create the IGBT/BRT by integration of the IGBT and BRT unit cells (Figure 2-2). The IGBT/BRT can be fabricated in the same process as the IGBT. The structure consists of a basic four-layer vertical thyristor with an IGBT structure integrated in the N-drift region. The IGBT is used to supply electrons to the N-drift region to turn on the device, while the P-channel MOSFET is used to suppress the thyristor action. With both gates positively biased, the electron current supplied through the IGBT structure provides base-drive current for the PNP transistor. The holes collected by the P-base region flow under the N⁺ emitter to the cathode short located orthogonal to the cross section. This results in forward-biasing of the N⁺/P- base junction and triggering of the thyristor. Under these conditions, the IGBT/BRT has the excellent on-state characteristics of a thyristor, including high surge current handling capability. When the IGBT gate (Gate 1) is positively biased and the BRT gate (Gate 2) is negatively biased, the P-base region is shorted to the cathode electrode through the P channel MOSFET. The holes collected in the P-base region can be shunted via the lateral P channel MOSFET, suppressing latch-up of the thyristor. The device operation now resembles an IGBT in its on-state, except that there is a P channel MOSFET in series with the vertical PNP bipolar transistor. In this IGBT mode, the IGBT/BRT exhibits good FBSOA, which can be utilized for controlled turn-on and short-circuit functions. With both gates negatively biased, the device is off. The on-state provides parallel current paths for transient hole current through the BRT diverter and the IGBT collector. This will improve the maximum controllable current over the IGBT, with the capabilities of a low on-state voltage drop of the BRT device and the added FBSOA of the IGBT. When both gates are shorted to the cathode terminal, the device can support a high forward blocking voltage across the reverse-biased P base/N⁻ drift region. When compared with DGBRT, there is a built-in IGBT structure, which will improve the SOA capability of the device [10].

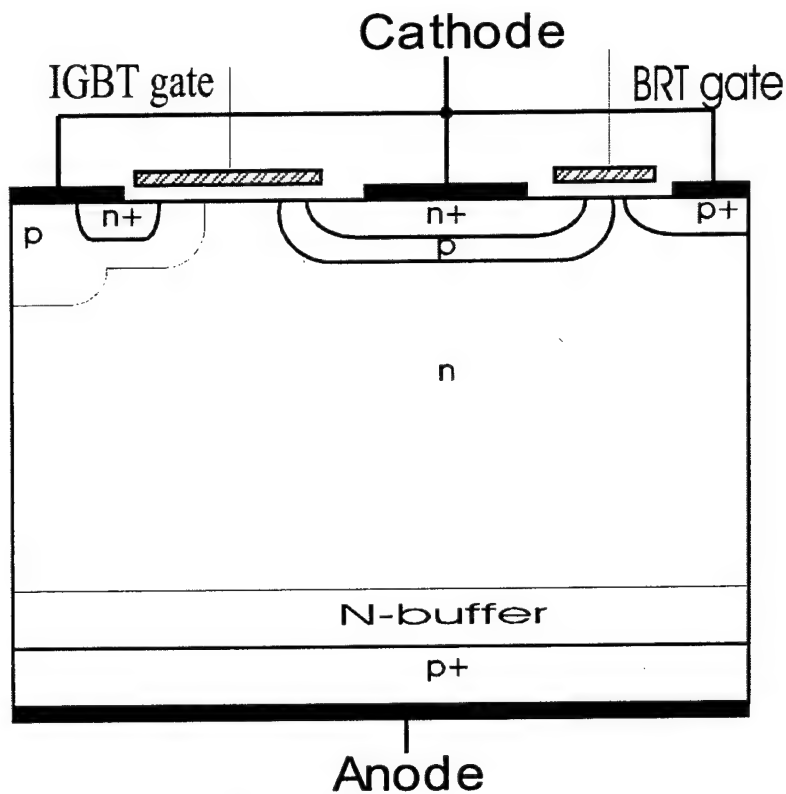


Figure 2-2. Schematic cross-section of the IGBT/BRT structure.

As shown in Figure 2-3, the IGBT/BRT introduces a transient IGBT operation between the on-state and the off-state. The IGBT/BRT is turned on in the IGBT mode by applying negative voltage to the BRT gate and positive voltage to the IGBT gate. After some delay, the voltage for the BRT gate is changed to positive or zero, so that during the on-state, the IGBT/BRT is operated in thyristor mode with a low forward voltage drop. There is a delay time of t_d before the turn-off signal arrives; the voltage on the BRT gate is changed to negative again to change the device operation mode from thyristor to transient IGBT mode. The device is then turned off like an IGBT by applying a negative voltage to the IGBT gate. During this transient time period, the forward voltage of the device will increase; however, since the transient state only accounts for a small percentage of the forward conduction time, the extra conduction loss caused by the increase of forward voltage drop is small. By adjusting the timing of the thyristor mode and the IGBT mode, the IGBT/BRT can improve the trade-off between the forward voltage drop and turn-off time to reduce the turn-off loss.

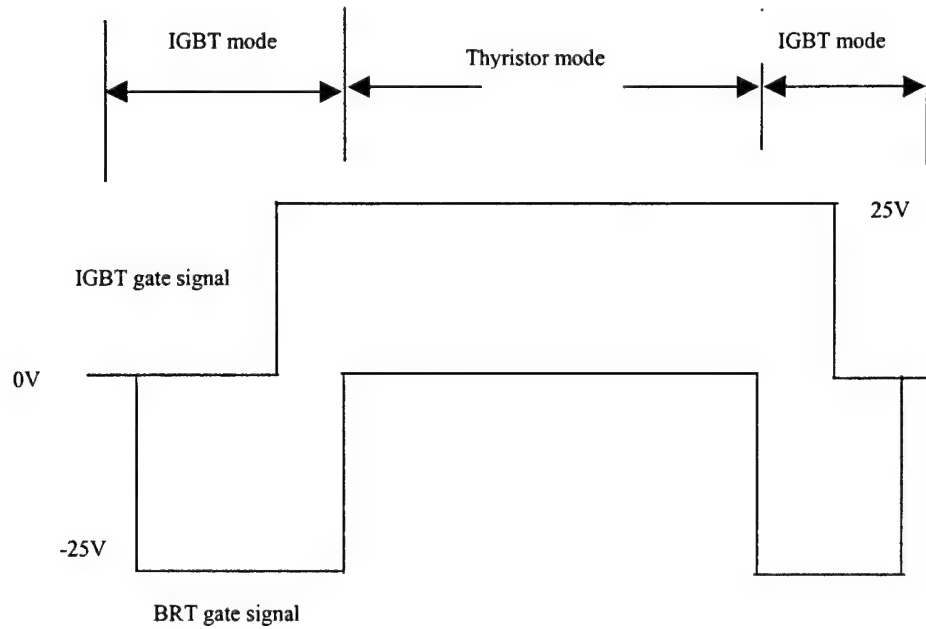


Figure 2-3. Waveform for the gate signals.

2.2.4 Scaled-up ALL-IGBT

The atomic lattice layout IGBT (ALL-IGBT) is a popular design due to its good latch-up immunity. For this project, an attempt was made to scale up the area of ALL-IGBT to obtain a current rating of 25A. Due to the suboptimal design, the design goal was not met.

2.3 ANALYSIS OF DEVICE OPERATION

2.3.1 TSOX-MPS RECTIFIER

2.3.1.1 Breakdown Voltage

When a reverse voltage higher than breakdown voltage is applied to a p - n junction, the junction breaks down and conducts a very high current. The breakdown voltage of the TSOX MPS rectifier is mainly determined by the p - n junction in the structure.

Avalanche multiplication is the most important mechanism in junction breakdown for power silicon devices, since the avalanche breakdown voltage imposes an upper limit on the reverse bias of most diodes, the collector voltages of bipolar transistors, and on the drain voltage of MOS-gated devices.

From the avalanche multiplication analysis, analytical expression for the condition of avalanche breakdown of abrupt p - n junction is given by:

$$\int_0^W 1.8 \times 10^{-35} \left[\frac{qN_B}{\epsilon_s} (W - x) \right]^7 dx = 1$$

Equation 1

From this equation, the depletion region width at breakdown for abrupt junction can be obtained by:

$$W_m = 2.67 \times 10^{10} N_B^{-7/8}$$

Equation 2

The W_m plotted in Figure 2-4 is calculated by the Equation 2. The voltage distribution can be determined by integrating Poisson's equation:

$$V(x) = \frac{qN_B}{\epsilon_s} \left(W - \frac{x^2}{2} \right)$$

Equation 3

Using Equation 2 and Equation 3, the breakdown voltage of abrupt junction for the case of $x=W$ is to be given by:

$$V_B = 5.34 \times 10^{13} N_B^{-3/4}$$

Equation 4

The maximum electric field at breakdown, which occurs at $x=0$ is:

$$E_m = 4010 N_B^{1/8}$$

Equation 5

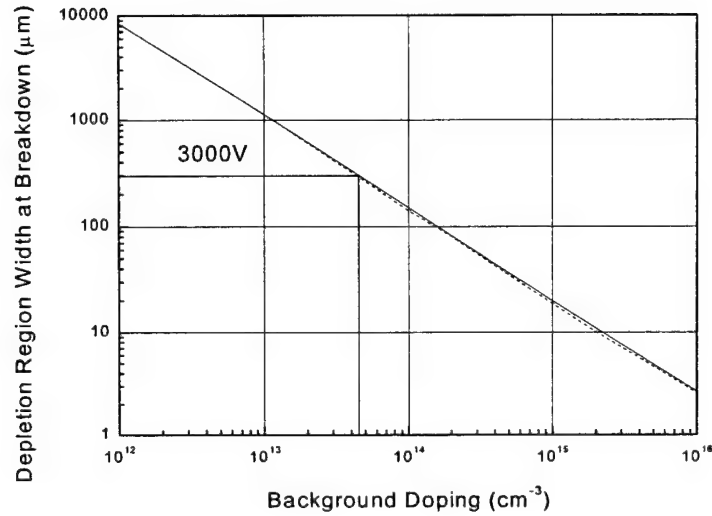


Figure 2-4. Depletion region width at breakdown for one-sided abrupt junction in silicon. The solid line represents the W_m according to Equation 2, and the dashed line represents the numerically calculated W_m .

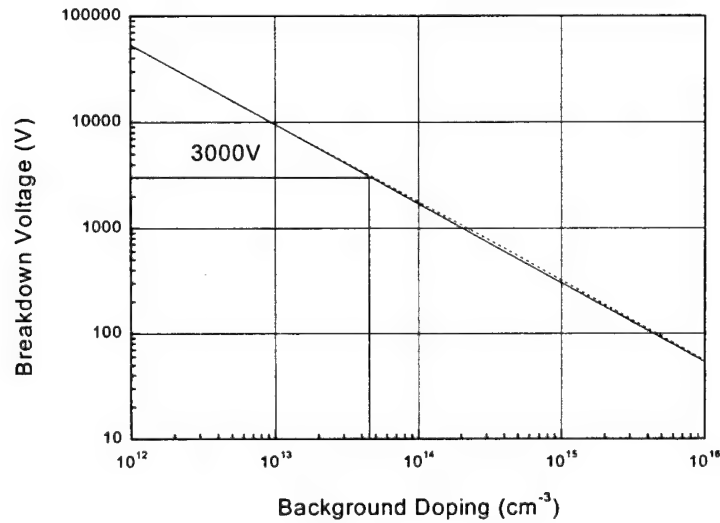


Figure 2-5. Avalanche breakdown voltage versus base doping for abrupt junctions in silicon. Solid line from Equation 4, dashed line from numerical calculation.

Other than the analytical approach, the depletion layer boundary at avalanche breakdown also can be determined by using the numerical iteration method. After calculation of W_m , which satisfies the ionization integral equation numerically, breakdown voltages are obtained by substituting W_m into Equation 3. The calculated values of maximum depletion-layer width at breakdown are shown in Figure 2-4. Figure 2-5 shows the analytically and numerically calculated value of the avalanche breakdown voltage of the abrupt junction at different background doping concentrations.

The analytical expressions allow the determination of the background doping level and the minimum base width required to achieve the breakdown voltage being designed for the high-voltage device. For the 3000V TSOX MPS rectifier, the minimum doping and width of the drift region is $4.6 \times 10^{13} / \text{cm}^3$ and, 293 μm , respectively. In practice, the device shows lower ideal breakdown voltage, owing to the imperfection of the edge termination. Especially in the TSOX MPS rectifier, the trench structure causes the high electric field at the edge of the trench, which leads to premature breakdown. For this reason, the device must be designed with lower doping and wider drift region than in the ideal case. In this analysis of the device, the base doping and the drift region width are assumed as $3 \times 10^{13} / \text{cm}^3$ and 300 μm , respectively.

2.3.1.2 Forward I-V Characteristics

2.3.1.2.1 Introduction

When a diode is forward-biased, it begins to conduct current. An ideal rectifier would be one that conducts a desired amount of current without the expense of forward voltage. In a real rectifier, however, there is usually a barrier and as well as resistance to the flow of current. In order for the current to flow, this barrier (and resistance) must be overcome by the application of electromotive force i.e., forward voltage. The on-state voltage is then a measure of the barrier (and resistance if any) to the flow of current. It follows then that a good rectifier must have minimal on-state voltage drop.

The Schottky barrier height must be lower than that of the p - n junction barrier height for the TSOX-MPS rectifier to have better forward conduction than the p - i - n junction

rectifier. When the TSOX-MPS rectifier is forward-biased, the potential barrier for thermionic emission over the Schottky barrier decreases since the Schottky junction is forward-biased, which results in increased current flow due to majority carrier injection. In this case, at low forward-bias voltages, the current through the diode is dominated by the current flowing through the Schottky region. At higher forward-bias voltages, the *p-i-n* junction would start injecting minority carriers, thereby modulating the drift region conductivity. This in turn greatly enhances the forward conduction of the Schottky diode, since the drift series resistance is greatly reduced. The current density at which the injection from the *p-i-n* junction becomes dominant depends upon the doping and thickness of the drift region. For a 400V TSOX-MPS rectifier, in which the doping is around $5 \times 10^{14}/\text{cm}^3$ and the thickness is $40\mu\text{m}$, the Schottky contact continues to carry most of the current even at current densities of $100\text{A}/\text{cm}^2$, which makes the TSOX-MPS rectifier better than both the *p-i-n* and Schottky rectifiers during forward conduction. As the resistance of the drift region increases, this current density becomes smaller. In the case of the 3000V device, the current density at which the injection from the *p-n* junction becomes dominant occurs at approximately several amperes per square centimeter. Thus, in designing the high voltage rating TSOX-MPS rectifier, a higher *p-i-n*-to-Schottky ratio is preferred.

The drift region parameters (doping and thickness) are determined by the reverse-blocking voltage requirements. The trench depth has marginal effect on the forward conduction characteristics since it affects neither the Schottky barrier height nor the *p-i-n* injection. Also, for a given total area of the diode, only the ratio of the *p-i-n* to Schottky area is important. This leaves three parameters that influence the forward conduction: (1) ratio of *p-i-n*/Schottky widths; (2) Schottky metal barrier height; (3) ambipolar lifetime in the drift region.

2.3.1.2.2 Forward characteristics as a function of Pin/Schottky Ratio

Let us now examine the effect of change in *p-i-n* to Schottky region widths on the forward voltage drop. The forward characteristics of the rectifiers with different *p-i-n* to Schottky ratios are shown in Figure 2-6.

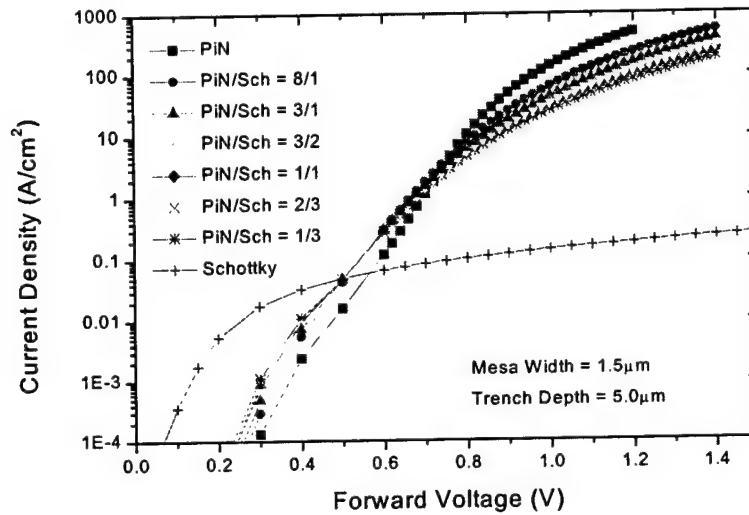


Figure 2-6. Simulated forward I-V characteristics of the 3000V TSOX-MPS rectifier as a function of *p-i-n* area to Schottky area ratio.

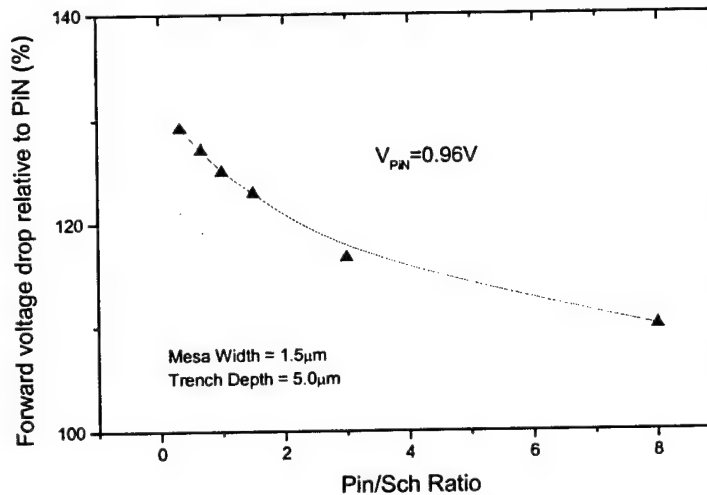


Figure 2-7. Relative forward voltage at 100A/cm² as a function of *p-i-n* to Schottky region width ratio

At low voltages the rectifiers with greater Schottky area carry more current because the series resistance of the drift region can be neglected at these current levels and the barrier against the current determines the forward voltage. The Schottky contact has a lower barrier than the *p-n* junction, most of the current flows through the Schottky contact.

At higher currents the series resistance of the *n*⁻ region becomes more important. As the forward bias is increased, the *p-i-n* region begins to inject holes and electrons into the drift region, modulating the conductivity of the drift region. The conductivity modulation is not limited to the *p-i-n* region, so the whole drift region is filled with electrons and

holes. In the TSOX-MPS rectifier, since the distance between two adjacent p^+ regions is much smaller than the diffusion length of the carriers, the carrier concentration in the drift region below the Schottky region is almost indistinguishable from that at the $p-i-n$ region. This also makes the TSOX-MPS rectifiers with different $p-i-n$ to Schottky ratios behave the same at current densities where conductivity modulation of the drift region is important. This high-level injection in the drift region also reduces the series resistance of the Schottky diode, making it appear like a low-voltage Schottky diode with low forward drop for higher current densities. Hence the TSOX-MPS rectifier has a lower forward drop than the $p-i-n$ rectifier at current densities higher than several amperes per square centimeter.

At still higher current densities, the drift region resistance becomes the only factor that influences the forward voltage. Since the TSOX-MPS rectifier has a lower level of conductivity modulation at these current densities, the $p-i-n$ junction rectifier begins to have a lower forward drop, and the difference between rectifiers with different $p-i-n$ -to-Schottky ratios again becomes conspicuous. For low voltage devices, the current density where the injection from the $p-i-n$ junction becomes the main component of the conduction current can be as high as $100\text{A}/\text{cm}^2$, whereas for high-voltage rating devices, the $p-i-n$ becomes dominant at a current density of several amperes per square centimeter. As shown in Figure 2-7, the differences of the forward I-V characteristics between devices with different $p-i-n$ -to-Schottky ratio are quite obvious at the range of practical conducting current density.

2.3.1.2.3 Forward characteristics as a function of Schottky barrier height

Figure 2-8 shows the forward characteristics of the 400V TSOX-MPS rectifiers with the same geometry, but different Schottky barrier heights. The $p-i-n$ and Schottky characteristics are included for comparison. It can be seen that the barrier height is more important at lower forward-bias currents. This is because the current is due to thermionic injection and there is insignificant minority carrier injection. Hence at lower current levels, the rectifiers with lower Schottky barrier height have a lower forward drop. At higher current levels, the conductivity modulation of the drift region is vital for current flow. In the case of higher voltage rating devices, in which the resistance of the drift

region is large, the effects of the Schottky barrier height are not obvious even in the range of low current density.

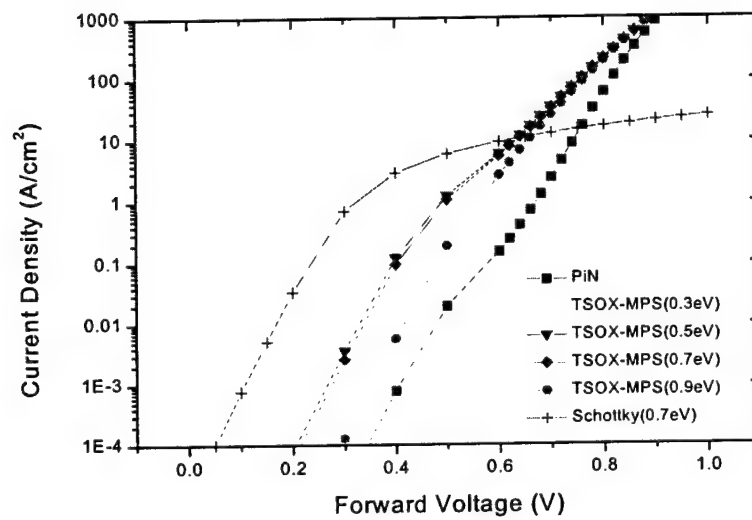


Figure 2-8. Simulated forward I-V characteristics of the 400V TSOX-MPS rectifier as a function of Schottky barrier height.

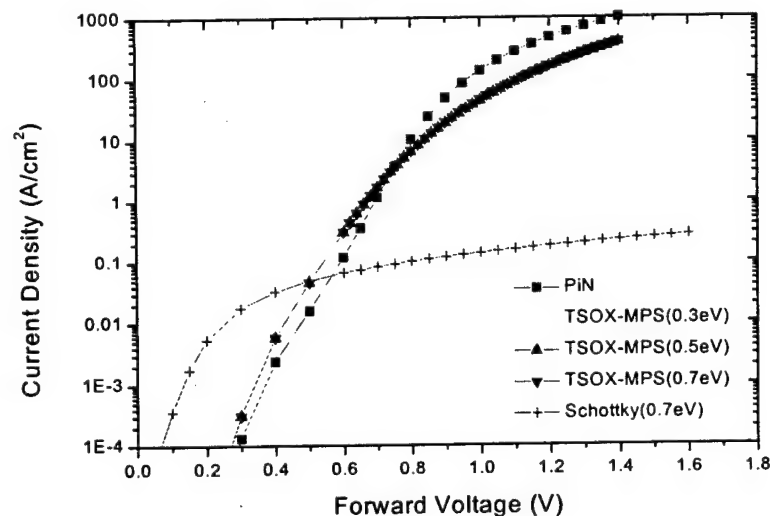


Figure 2-9. Simulated forward I-V characteristics of the 3000V TSOX-MPS rectifier as a function of Schottky barrier height.

2.3.1.2.4 Forward characteristics as a function of carrier lifetime

As the lifetime decreases, the carriers recombine faster and the conductivity modulation of the high resistive drift region is reduced and this in turn increases the forward drop. Figure 2-10 shows the forward I-V characteristics of the TSOX-MPS rectifiers with different high-level lifetimes. As expected, at low current densities, the forward I-V

characteristics are independent of the lifetime, since the Schottky diode dominates at these current levels. At higher current densities, the characteristics of the TSOX-MPS rectifiers with different lifetimes split, and higher lifetimes result in lower forward drops. As soon as the drift length of the carrier becomes comparable with the thickness of the drift region, the reduction of the forward voltage drop will become slower, since at this point most of the drift region is already conductivity modulated. This trend is clearly shown in Figure 2-11.

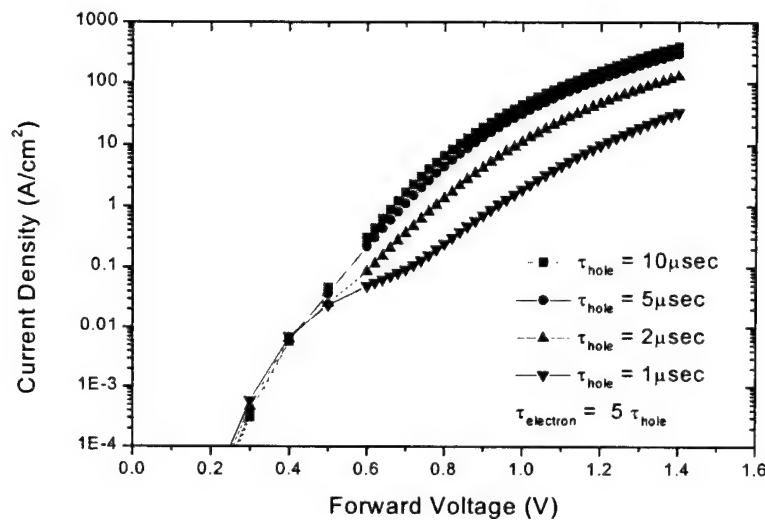


Figure 2-10. Forward characteristics of the 3000V TSOX-MPS rectifier as a function of ambipolar lifetime.

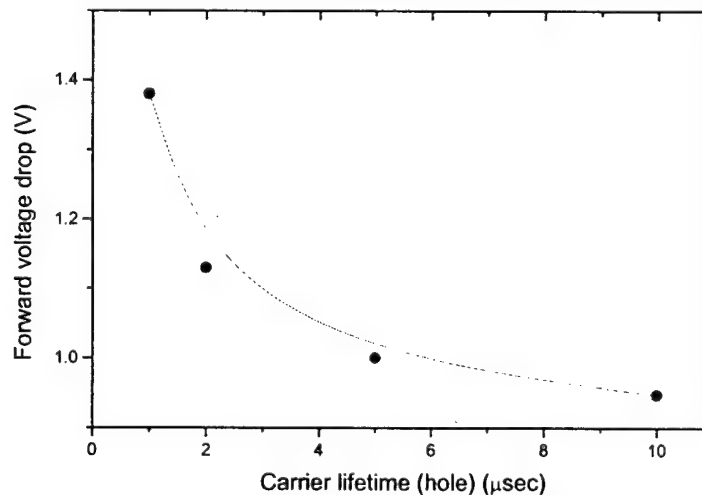


Figure 2-11. Forward voltage drop of the 3000V TSOX-MPS rectifier as a function of ambipolar lifetime.

2.3.1.3 Reverse I-V Characteristics

2.3.1.3.1 Introduction

Instead of assuming the TSOX-MPS rectifier to be a parallel combination of the $p-i-n$ and Schottky, one can treat it as a field-effect transistor, with a Schottky junction at the source and the gate shorted to the source. This representation is very useful for understanding the reverse-blocking characteristics of the TSOX-MPS rectifier. With the Schottky region totally depleted at equilibrium, the MOSFET is a normally-off transistor. Hence, when reverse voltage is applied, the voltage is supported by the depleted drift region under the Schottky junction rather than the Schottky junction. Since the potential of the Schottky junction remains constant regardless of the magnitude of the cathode bias, the leakage current is essentially due to generation in the space charge region, which is equal to the $p-i-n$ junction reverse leakage.

The breakdown voltage (BV) of the rectifier is determined by three factors, namely drift region doping, drift region thickness and termination efficiency. The termination efficiency depends on the type of termination used and its design. It is possible to achieve termination efficiencies over 90% using a combination of floating field regions and field plate.

Having determined the appropriate drift region doping and thickness, the next step is to design for minimum leakage current. The reverse leakage current of the TSOX-MPS rectifier depends on the ability of the $p-i-n$ region to shield the Schottky junction. It thus depends on the distance between adjacent $p-i-n$ regions (the Schottky region width) and the depth over which the $p-i-n$ junctions shield the nearby Schottky contact, i.e., the trench depth. When the shielding is not perfect, part of the voltage has to be supported by the Schottky region, then the Schottky barrier also becomes important.

2.3.1.3.2 Reverse leakage current as a function of Schottky Barrier Height

The TSOX-MPS rectifier is designed so that when in equilibrium, the Schottky contact is completely isolated from the region that supports the reverse bias. Since the Schottky contact never supports any voltage, it follows that the reverse blocking characteristics are

independent of the Schottky barrier height. Simulation results in Figure 2-12 clearly verify this view.

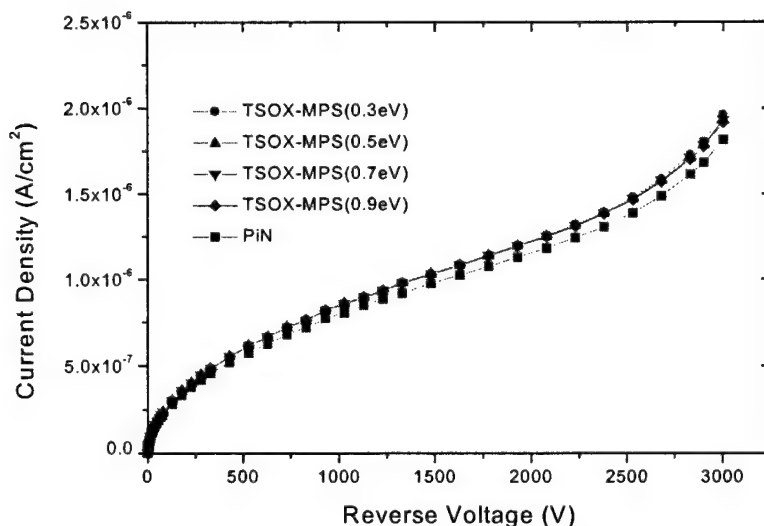


Figure 2-12. Reverse leakage current of the 3000V TSOX-MPS rectifier as a function of Schottky barrier height.

2.3.1.3.3 Reverse leakage current as a function of mesa width

We now examine the reverse blocking characteristics that result in changes to the mesa width. When the mesa width is increased, the Schottky region is less effectively controlled by the $p-i-n$ region. As the reverse-bias is increased, part of the field lines from the depletion charge in the Schottky region terminate at the cathode. In other words, part of the channel is now controlled by the cathode (drain of the MOSFET). This results in the lowering of the barrier between the cathode and the anode, similar to a short-channel MOSFET. Since in the TSOX MPS rectifier we have a cathode instead of the drain we refer to this phenomenon as cathode-induced barrier lowering (CIBL). The CIBL results in a steep increase in leakage current with reverse-bias beyond some voltage at which the barrier lowering is significant. In a MOSFET a channel is short or not, depending on whether the gradual channel approximation holds. Intuitively a channel is long if the gate is in control of the channel, and the channel is short if the drain bias significantly affects the drain current in saturation. Hence, in this case, the CIBL depends on the length of the Schottky region (MOSFET channel) as well as the distance between the two gates and the oxide thickness. The oxide thickness is fixed from process considerations. We can then come up with two ways to overcome CIBL. Either make the channel longer, i.e. increase

trench depth, or put the *p-i-n* (gate) regions closer, i.e., reduce the mesa width. Greater trench depths imply a longer MOSFET channel. Since the channel length of the MOSFET is now longer, the short-channel effect (CIBL) is less pronounced.

Figure 2-13 and Figure 2-14 show the reverse blocking characteristic of TSOX-MPS rectifiers with different mesa width. Evidence of a clear dependence of leakage current upon the mesa width is demonstrated in these simulation results. Figure 2-14 shows that to limit the leakage within 10 times of that of the *p-i-n* rectifier, the aspect ratio of the mesa should be less than 1.

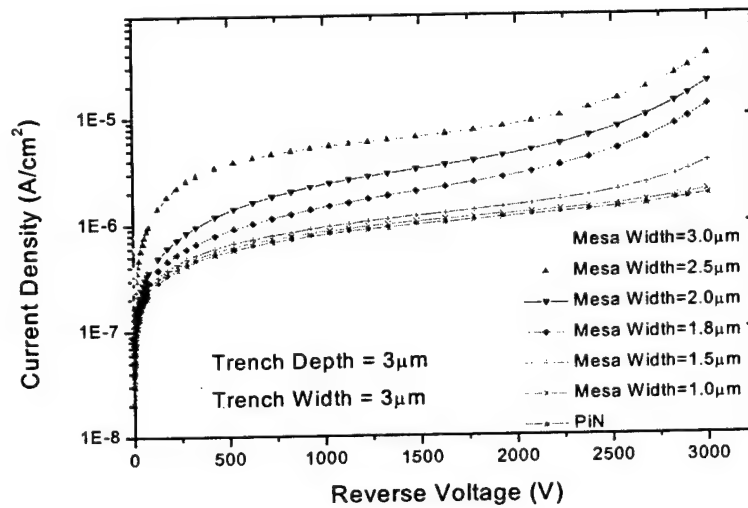


Figure 2-13. Reverse blocking characteristics of the TSOX-MPS rectifier as a function of mesa width.

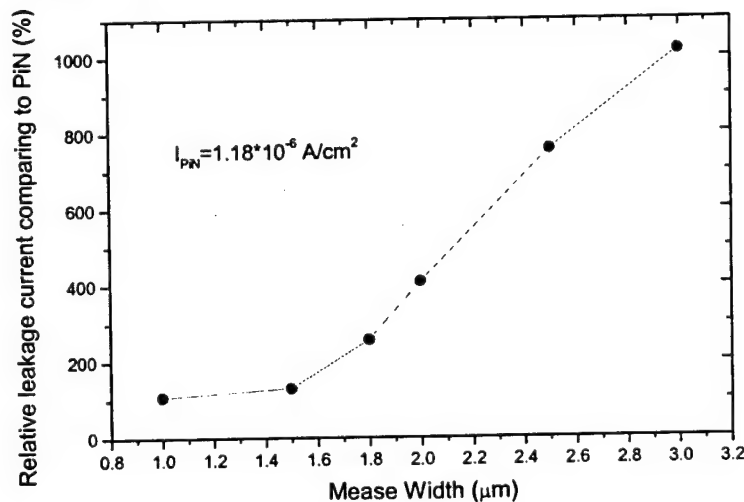


Figure 2-14. Reverse blocking characteristics of the TSOX-MPS rectifier as a function of mesa width.

2.3.1.4 Switching Characteristics

While switching the rectifier from its forward conduction state to its reverse blocking state, all the stored charge in the device has to be removed. In the TSOX-MPS rectifier, during the turning-off, while the holes are moved through the p^+ region, as long as the Schottky region is forward-biased over its barrier height, thermionic electrons are still injected across the Schottky barrier, which results in reduced total current. This phenomenon, along with the fact that there is lesser stored charge in the TSOX-MPS compared to the $p-i-n$ rectifier at the same current level, results in much better switching characteristics. Figure 2-15 shows the simulation results of the reverse recovery characteristic of TSOX-MPS rectifiers with different $p-i-n/Sch$ ratios. The switching characteristics of the $p-i-n$ rectifier are included for comparison. It is clear that peak reverse current density and turn-off time is greatly reduced with the trench MPS structure.

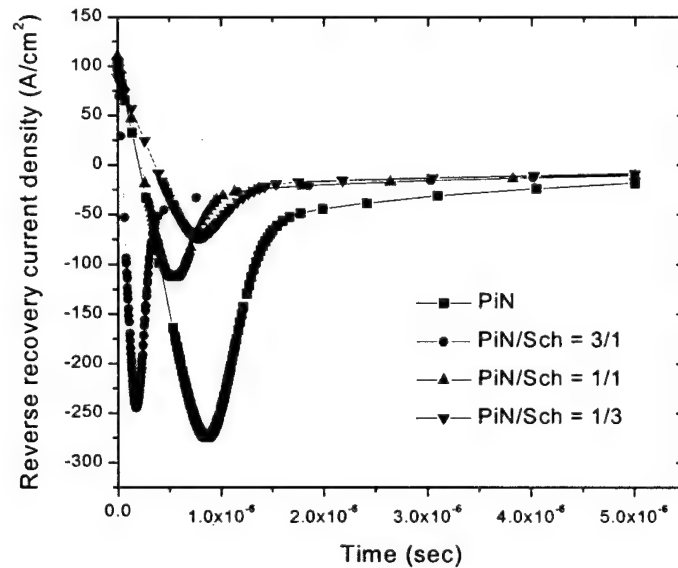


Figure 2-15. Reverse recovery characteristics of the 3000V TSOX-MPS rectifier as a function of different $p-i-n$ to Schottky ratios.

Figure 2-16 shows the trade-off curve between the forward voltage drop and the turn-off time t_{off} . Here, t_{off} is defined as the time when the reverse current decreases to 25% of its peak value. It can be clearly seen that the switching performance is greatly improved. For the same carrier lifetime, the turn-off time is decreased approximately by a factor of four. Figure 2-17 shows the trade-off curve between forward voltage drop and the stored

charge density, which again verifies the improvement of the device characteristic over the traditional *p-i-n* rectifiers.

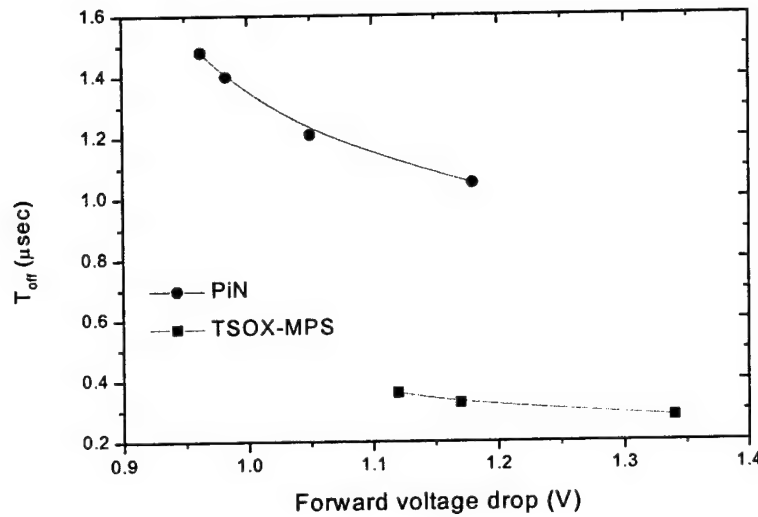


Figure 2-16. Trade-off curve of the 3000V TSOX-MPS rectifier (V_f vs. T_{off}).

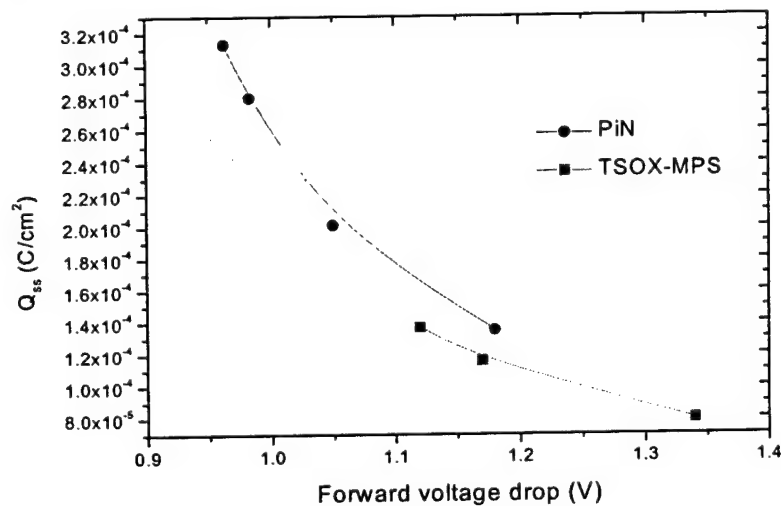


Figure 2-17. Trade-off curve of the 3000V TSOX-MPS rectifier (V_f vs. Q_{ss}).

2.3.1.5 Reverse Leakage Current Model of the TSOX-MPS Rectifier

2.3.1.5.1 Introduction

Figure 2-13 shows that the reverse current slopes at $1\mu\text{m}$ mesa width and $3\mu\text{m}$ mesa width are the same. We expect that the reverse current of the $3\mu\text{m}$ mesa device shows the higher current slope because of less pinch-off effect and higher electric field at the Schottky contact compared to that of $1\mu\text{m}$ mesa device. This erratic calculation is

attributed to the MEDICI Schottky model. The MEDICI model of the Schottky contact does not take into account the CIBL, the Schottky barrier lowering effect. This imperfection of the MEDICI model was a motivation to develop the more accurate analytic model.

The Schottky contact is located on the top of the mesa, which is depleted when reverse voltage is applied to the anode of the TSOX MPS rectifier. The trenches adjacent to the mesa are filled by highly doped and highly conductive polysilicon so that the potential of the whole sidewall of the mesa becomes zero. This boundary condition enables the mesa region to be pinched off effectively. Assuming that the whole mesa region is completely depleted, the potential in the mesa can be calculated by Poisson's equation. The deep conductive trenches aside act as a corona cage that shield the electric field at the mesa so that it is reduced. This shielding effect, causing low electric field at the Schottky contact at the top of the mesa, relieves the Schottky barrier lowering effect and consequently reduces the reverse leakage current at the Schottky junction.

$$\Delta\phi_b = \sqrt{\frac{qE}{4\pi\epsilon_s}} + \alpha E$$

Equation 6

Other than the Schottky contact, the space-charge region in the middle region of the TSOX MPS rectifier also generates reverse leakage current. This leakage current mainly depends on the space-charge generation lifetime, which is the function of the minority carrier lifetime and the amount of energy in the deep level. This parameter has been measured from the reverse leakage current of the p-i-n rectifier on the same wafer on which the TSOX MPS was fabricated. Carrier diffusion at the neutral region also causes the reverse leakage current of the TSOX MPS rectifier as well. The carriers generated within the diffusion length to the depletion boundary are collected in the depletion area and swept by an electric field in the depletion region. However, the diffusion current in the silicon *p-n* junction diode is several orders lower than that of the space-charge generation current at the reverse-bias. Taking into account the two major reverse leakage current components, the reverse leakage current model of the TSOX MPS rectifier was

developed. It was proven that the results of the model calculation match the actual reverse I-V curve.

2.3.1.5.2 Analytic model of the reverse current of TSOX MPS rectifier

The trench and mesa structure of the TSOX MPS are illustrated in Figure 2-18. The base doping of the epi-layer is $3 \times 10^{13}/\text{cm}^3$. The trench is filled with heavily doped polysilicon. The sidewall oxide is between the polysilicon and mesa silicon to form a MOS structure. The heavily doped polysilicon is considered a conductor in this model. The top of the mesa is defined as a Schottky contact. The Schottky contact and the polysilicon are shorted to have ground potential. The mesa is assumed to be completely depleted. Before the onset of the strong inversion, the potential in the mesa region is

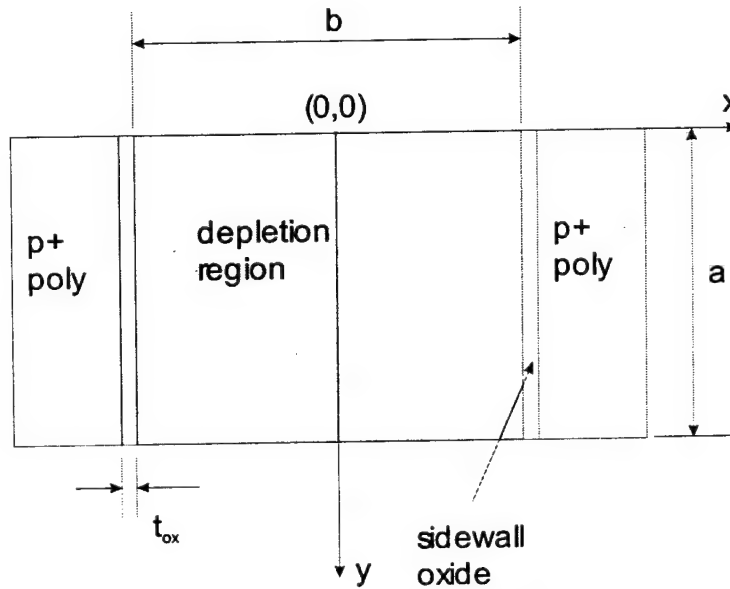


Figure 2-18. The coordination system at mesa area of the TSOX MPS rectifier.

$$\frac{\partial^2 \Phi(x, y)}{\partial x^2} + \frac{\partial^2 \Phi(x, y)}{\partial y^2} = -\frac{\rho}{\epsilon_s}$$

$$-\frac{b}{2} \leq x \leq \frac{b}{2}, 0 \leq y \leq a$$

Equation 7

where ρ is the charge density in the mesa region and ϵ_s is the dielectric constant of silicon. The ρ will be the charge density formed by doped impurities in this region.

The solution of the Equation 7 as a function of only y is a hyperbolic or exponential function such as

$$\Phi_1(y) = k_1 \cosh(\lambda y) + k_2 \sinh(\lambda y) - \gamma,$$

Equation 8

where

$$\lambda^2 = \frac{2}{\left(1 + 2 \frac{C_{si}}{C_{ox}}\right) \left(\frac{b}{2}\right)^2} s$$

$$\gamma = \beta/\lambda^2, \text{ and}$$

$$\beta = \frac{-qN_B}{\epsilon_s} + \frac{\phi_{ms} - \frac{Q_t}{C_{ox}}}{\left(1 + 2 \frac{C_{si}}{C_{ox}}\right) \left(\frac{b}{2}\right)^2}$$

where the N_B is the background doping, ϵ_s is the dielectric constant, ϕ_{ms} is the workfunction difference between the metal and the semiconductor, C_{si} is the capacitance of the mesa and C_{ox} is the capacitance of sidewall oxide. The constants k_1 and k_2 can be obtained with the boundary values $\Phi_1(0)$ and $\Phi_1(a)$ at $y=0$ and $y=a$, respectively:

$$\begin{aligned} k_1 &= \Phi_1(0) + \gamma \\ k_2 &= \frac{\Phi_1(a) + \gamma - (\Phi_1(0) + \gamma) \cosh(\lambda a)}{\sinh(\lambda a)} \end{aligned}$$

Equation 9

The complete solution for potential is given by

$$\Phi(x, y) = \Phi_1(y) \left(1 - \frac{(\lambda x)^2}{2}\right)$$

Equation 10

Figure 2-19 shows the three-dimensional view of potential distribution in the mesa calculated by Equation 10. One-dimensional potential distribution along the center of the mesa calculated by the Equation 8 with various mesa aspect ratios is shown in Figure

2-20. As expected, the graph shows the high aspect ratio of the mesa gives more effective potential shielding.

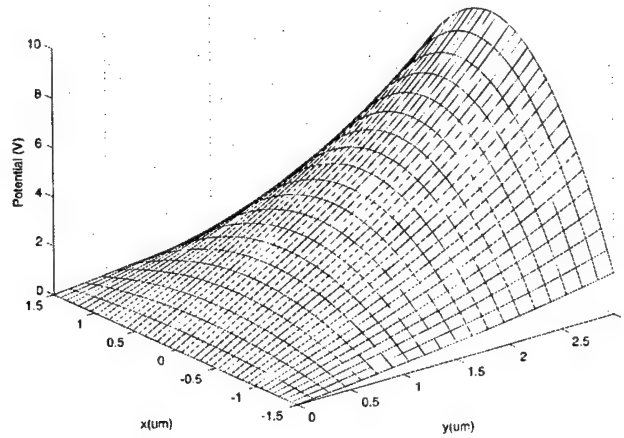


Figure 2-19. Potential distribution in the mesa with at $a=3\mu\text{m}$, $b=3\mu\text{m}$, and $\Phi_1(a)=10\text{V}$.

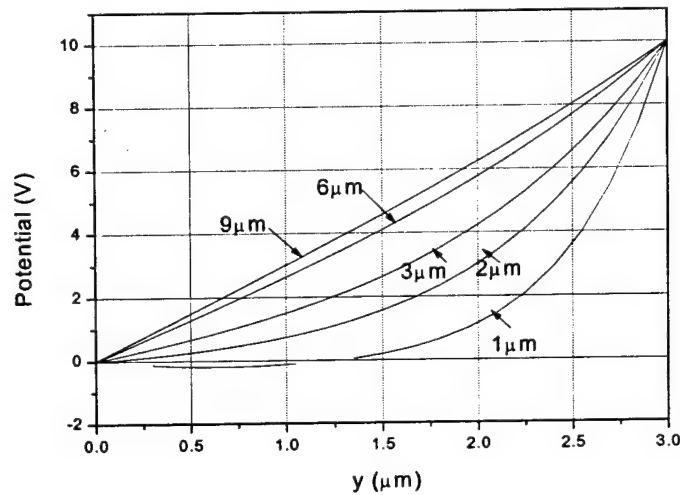


Figure 2-20. Potential distribution in the mesa with various aspect ratio at $a=3\mu\text{m}$, $b=1, 2, 3, 4, 6, 9\mu\text{m}$, and $\Phi_1(a)=10\text{V}$.

The electric field at the top surface of the mesa causes the Schottky barrier to be lowered. The derivative in y of the Equation 10 gives the electric field on the mesa surface, such that

$$E_y(x)\Big|_{y=0} = k_2 \lambda \cdot \left(1 - \frac{x^2}{\left(1 + \frac{2C_{Si}}{C_{ox}} \right) \left(\frac{b}{2} \right)^2} \right)$$

Equation 11

The electric field at the Schottky contact on the mesa is shown in Figure 2-21. The electric field is at its maximum at the center of the mesa and its minimum at the edges of the mesa. It can be the reverse current at the Schottky contact.

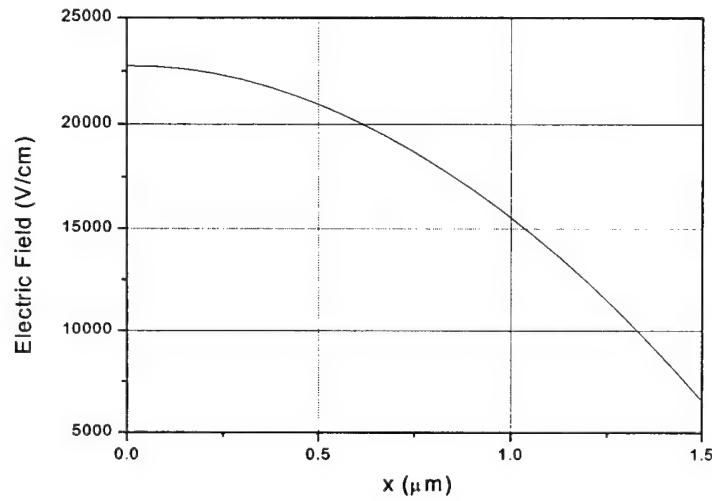


Figure 2-21. Electric field on the mesa top at $a=3\mu\text{m}$.

The lowering of the Schottky barrier is also a function of x , and the saturation current is given by

$$J_s = \frac{A^{**} T^2}{b} \exp\left(-\frac{q\phi_b}{kT}\right) \int_0^b \exp\left(\frac{q\Delta\phi_b(x)}{kT}\right) dx,$$

Equation 12

where the A^{**} is Richardson's constant, T is the Kelvin temperature, q is the electron charge, ϕ_b is the Schottky barrier height, and $\Delta\phi_b$ is the barrier lowering given in Equation 6

At the reverse-bias condition, the depleted region width increases with the reverse voltage. Most of the drift region of rectifiers are depleted, including the punch-through

rectifiers. Once the neutral region is depleted, the deep level behaves as a generation center. The generation rate is known as inverse of space-charge lifetime τ_{sc} [8]. The space-charge lifetime is given by

$$\tau_{sc} = \tau_{po} \exp\left(\frac{E_r - E_i}{kT}\right) + \tau_{no} \exp\left(\frac{E_i - E_r}{kT}\right)$$

Equation 13

where the τ_{po} is the hole lifetime, τ_{no} is the electron lifetime, E_r is the trap energy level, and E_i is the intrinsic energy level. The τ_{sc} can be calculated when the minority carrier lifetime and energy of the deep level are known. This generation center could be formed during device fabrication processes due to crystal defects by ion implant or RIE, contamination by heavy ions, and so on. The energy levels and densities of the deep energy level are not evaluated separately. Without measuring the minority carrier lifetime and deep level, however, the τ_{sc} can be measured from the leakage current of the p-i-n rectifier. Assuming the uniform generation throughout the depletion region, the space-charge generation current is

$$J_{sc} = qn_i \int \tau_{sc}^{-1} dW,$$

Equation 14

where W is the width of the space-charge region. Combining Equation 12 and Equation 14, reverse I-V curves can be obtained which are shown in next section.

2.3.1.5.3 The reverse leakage current of TSOX MPS rectifier

Based on the analysis of the Schottky barrier lowering at mesa between trenches, and generation current at the space charge region, the reverse leakage currents of the TSOX MPS rectifier are calculated. Figure 2-22 shows the calculated reverse leakage current of the 3000V TSOX MPS rectifier. The current values in the graph are normalized values as the Schottky area out of the active area is unity. In this calculation, the trench depth is $3\mu\text{m}$, the Schottky barrier height is 0.79eV , thickness of the sidewall oxide is $0.1\mu\text{m}$, background doping is $5 \times 10^{13}/\text{cm}^3$, and the ϕ_{ms} is assumed to be 0.9eV . When the mesa width is $1\mu\text{m}$, the reverse current of the Schottky junction does not change with

increasing reverse voltage. That means the electric field at the Schottky junction is almost independent from the reverse voltage. As shown in Figure 2-20, for 1 μm mesa width, the penetration depth of external voltage is 1.5 μm which is one half of the trench depth. That is the external potential that cannot reach the top of the mesa. This shielding effect of the trench sidewall makes the electric field at the Schottky junction constant at any terminal voltage.

When the mesa width increases to 6 μm , the reverse current at reverse voltage of 3000V becomes 100 times that of the 1 μm mesa. Reverse current of the Schottky rectifier at 3000V is more than 10,000 times that of the 1 μm mesa TSOX MPS rectifier.

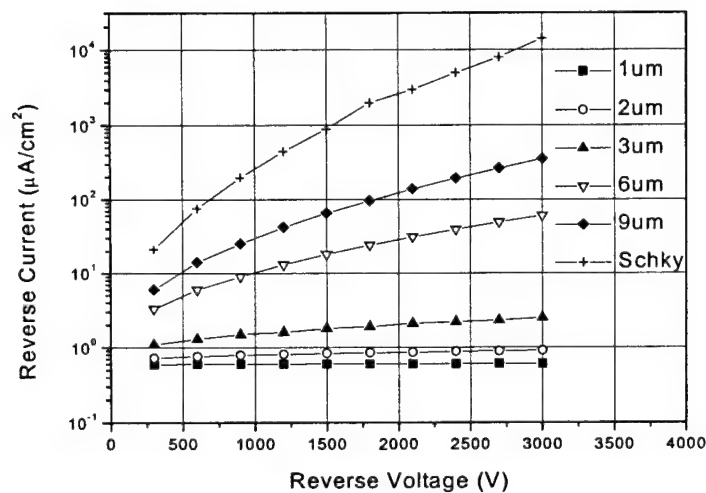


Figure 2-22. Reverse current curve for the TSOX MPS and the Schottky rectifier. For the TSOX MPS rectifier, the current curves represent the reverse current through the Schottky contact only so that compare the magnitude to that of Schottky rectifier.

With a conventional Schottky rectifier structure, the fabrication of the Schottky rectifier with reverse current as low as that of the *p-i-n* rectifier is not possible. It has been claimed that the TSOX MPS rectifier's reverse leakage current could reach the limiting value at minimum mesa width.

Figure 2-23 shows the reverse current of a TSOX MPS rectifier, which contains the Schottky reverse current and generation current in the depletion region at various mesa widths. In this calculation, the trench depth is 3 μm , the Schottky barrier height is 0.79eV, the thickness of the sidewall oxide is 0.1 μm , the background doping is $5 \times 10^{13}/\text{cm}^3$, and

the ϕ_{ms} is assumed to be 0.9eV. When the mesa width is around 1 to 2 μm , the reverse current of the TSOX MPS rectifier is close to that of the $p-i-n$ rectifier. At higher Schottky barrier heights, the reverse current of the TSOX MPS rectifier might be even less than that of the $p-i-n$ rectifier. In practice, however, the preparation of the ideal Schottky contact is not easy. That means the leakage current from the Schottky contact could be higher than calculated value. Figure 2-23 shows that the reverse current is not acceptable for mesa widths wider than 6 μm . The reverse current of the TSOX MPS rectifier is about 10 and 100 times that of the $p-i-n$ rectifier at 6 and 9 μm mesa widths, respectively.

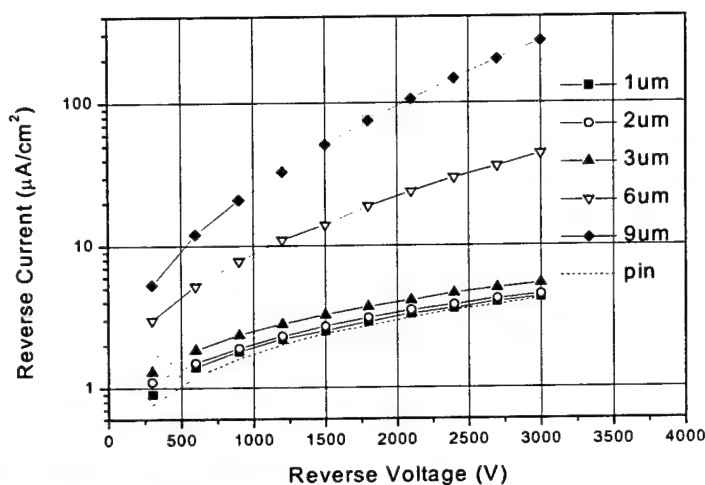


Figure 2-23. Reverse current curves for the TSOX MPS and the $p-i-n$ rectifier. For the TSOX MPS rectifier, the reverse current is the sum of the Schottky current component and the space-charge generation current component.

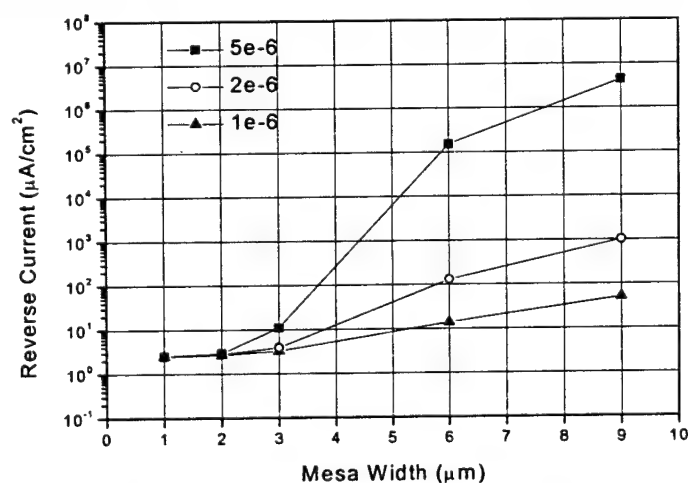


Figure 2-24. Reverse current of the TSOX MPS rectifier at 1500V reverse-bias and various mesa widths. The Schottky barrier height is 0.79eV, while α is 1×10^{-6} , 2×10^{-6} , and 5×10^{-6} .

Figure 2-24 shows the reverse current of the TSOX MPS rectifier when the reverse-bias is 1500V, the Schottky barrier height is 0.79eV, the trench depth is 3 μ m, and the background doping is 5 $\times 10^{13}$ /cm³. The three sets of curves represent the reverse current at three different α values. The reverse current of the TSOX MPS rectifier is invariant until the mesa width is 2 μ m at any value of α . The reverse current is very sensitive to the α value when α is higher than 3 μ m. The curves indicate that the mesa width is kept less than 3 μ m in order to control the reverse current consistently under inhomogeneous Schottky contact condition. The barrier height and α are the process-dependent. Actually, the thickness of the native oxide, cleanness of semiconductor surface and the uniformity of the silicide or metal interface with substrate are not under control in usual fabrication environments. These unexpected factors result in an inhomogeneous Schottky interface, the different barrier heights and α , device by device. Under this circumstance, the reverse current of the TSOX MPS rectifier can be maintained at the same value with the narrow mesa width. Figure 2-25 shows the reverse current at a condition similar to that of Figure 2-24. In this graph, the three sets of reverse currents represent three different Schottky barrier heights; α is fixed at 1 $\times 10^{-6}$. It should be noted that the lower mesa width allows easier control of the reverse current. The barrier height of 0.75 ~ 0.79eV is commonly acquired in the Al-Si Schottky contact, depending on the annealing temperature. The PtSi-Si Schottky contact shows the barrier height as high as 0.85eV. In a high-voltage Schottky rectifier, the PtSi was often used as a Schottky material because of high barrier height on the n^- type semiconductor. The graph implies that the PtSi might be the best material for TSOX MPS rectifier in terms of reverse current. The benefit of the high barrier height is that the reverse current is not much changed with the mesa width at a barrier height of 0.85eV.

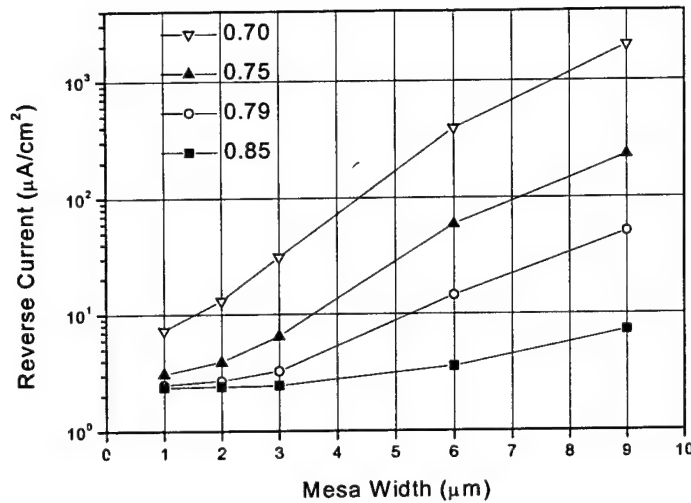


Figure 2-25. Reverse current of TSOX MPS rectifier at reverse bias of 1500V, and various mesa widths. The α is $1e-6$, while the Schottky barrier height is 0.70, 0.75, 0.79 and 0.85eV.

2.3.1.6 JTE termination for TSOX MPS rectifier

The active area of the TSOX MPS rectifier is bordered by the JTE termination. The surrounding area is also etched down to the same depth as the trenches in the active area. p -type ions implant lightly on the surrounding area, and successive diffusion forms the JTE termination. Figure 2-26 shows a cross-section of the JTE termination. The relationship between breakdown voltage and implant surface impurity concentration has been found by MEDICI simulation.

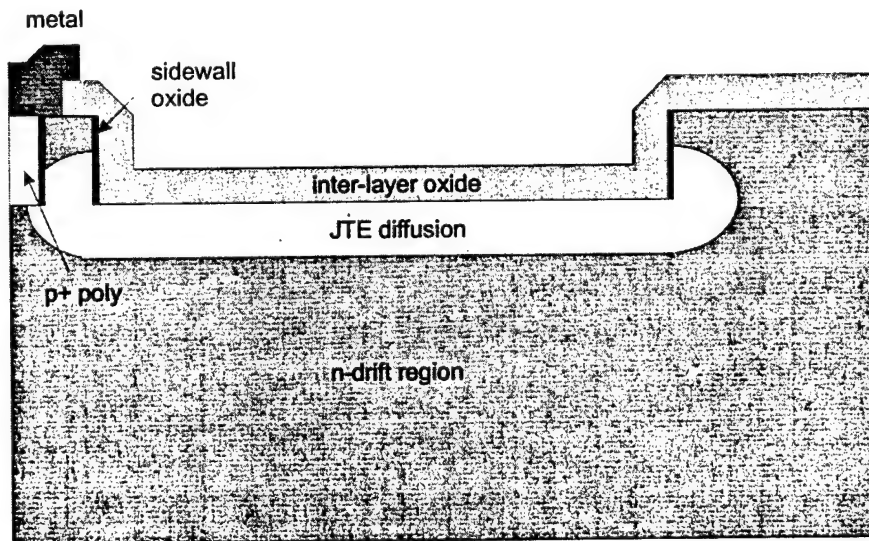


Figure 2-26. Cross-section of the termination of the 3000V TSOX MPS rectifier.

The device structure shown in Figure 2-26 was used as an input structure for the MEDICI simulation. Figure 2-27 shows the equi-potential line in the JTE region at 3000V reverse voltage. The JTE diffusion region is completely depleted at anode reverse voltage. Because the JTE region turns into a space-charge region at reverse-bias, the potential is distributed along the JTE termination. The voltage dividing action of the JTE reduces the potential drop at the main junction.

Figure 2-28 shows the blocking voltage of the TSOX MPS rectifier with the JTE termination at various JTE doping conditions. The breakdown voltage increases with increases in the surface charge density C_s until it reaches to $C_{s(max)}$. The value of the $C_{s(max)}$ in Figure 2-28 is $8.8 \times 10^{15}/\text{cm}^3$. Further increase of the C_s causes abrupt decrease of the blocking voltage. At lower surface charge than $C_{s(max)}$ on the JTE, the maximum electric field is focused on the main junction. Whereas, at surface charges higher than $C_{s(max)}$ on the JTE, the location of the maximum electric field moves to the edge of JTE termination. Optimization of the JTE can be achieved when the same peak electric fields are applied to the main junction and the edge of the JTE termination at full reverse voltage. As shown in Figure 2-28, the blocking voltage of the JTE termination changes with the surface doping at the fixed lateral length of the JTE termination. The maximum breakdown voltage of the termination could be obtained by controlling the implant dose so that the entire JTE area can be completely depleted at the peak reverse voltage.

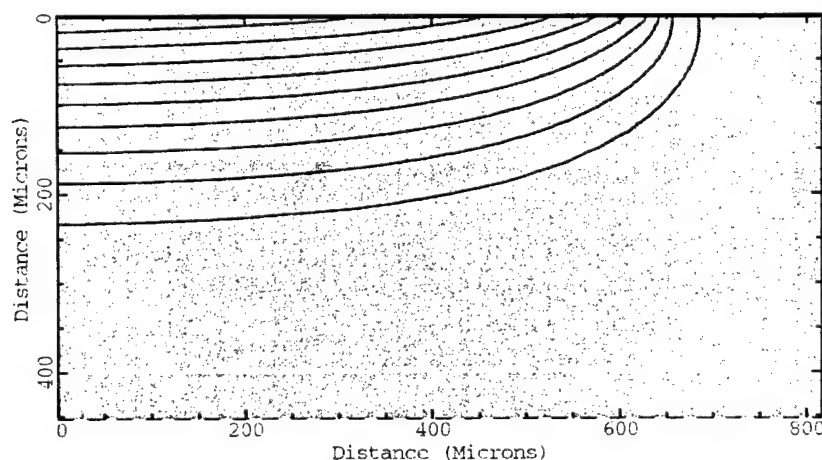


Figure 2-27. Equipotential line on the JTE termination. The shallow light gray area at the top of the structure is the JTE diffusion area.

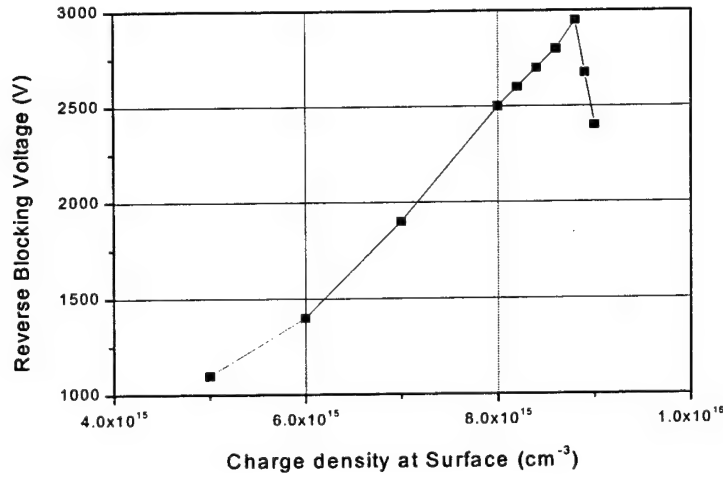


Figure 2-28. Relationship between the blocking voltage and the surface charge density of the JTE termination.

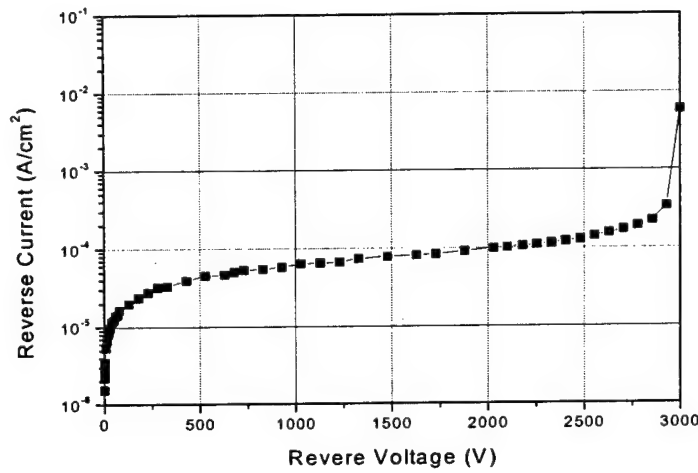


Figure 2-29. Reverse I-V curve of the 3000V TSOX MPS rectifier with JTE termination.

In order to fabricate the JTE termination, it is necessary to find the implantation dose of impurity. From the MEDICI calculation, the surface impurity density and the junction depth of JTE can be extracted at the point at which the maximum blocking voltage occurs, as shown in Figure 2-29. The impurity concentration density at the surface is $C(0) = C_s = 8.8 \times 10^{15} / \text{cm}^3$ and the junction depth is $x_j = 3.8 \mu\text{m}$.

The impurity concentration by diffusion from limited source is given by:

$$C(x,t) = \frac{S}{\sqrt{\pi Dt}} \exp\left(\frac{-x^2}{4Dt}\right),$$

Equation 15

where S is the amount of material placed on the surface prior to diffusion, D is diffusivity, and t is diffusion time. For a wafer of background doping of $3 \times 10^{13}/\text{cm}^3$, the impurity concentration at the junction x_j is $3 \times 10^{13}/\text{cm}^3$, or $C_s = 3 \times 10^{13}/\text{cm}^3$. At $C(x_j)/C_s = 3 \times 10^{13}/8.8 \times 10^{15} = 0.0034$

From Gaussian profile [3-1-15],

$$\frac{x}{2\sqrt{Dt}} = 2.35$$

Equation 16

or

$$\sqrt{Dt} = \frac{3.8 \times 10^{-4}}{2.35} = 8.09 \times 10^{-5}$$

Equation 17

for $x=x_j=3.8\mu\text{m}$.

From Equation 15 and Equation 17,

$$S = C_s \sqrt{\pi Dt} = 1.26 \times 10^{12} / \text{cm}^2$$

Equation 18

The most common method of pre-deposition of impurities on the wafer is ion implantation. The S is the implant dose of the JTE termination, which has been calculated to be $1.26 \times 10^{12}/\text{cm}^2$. It has been found that the junction depth of the JTE termination does not change the blocking voltage of the device.

2.3.1.7 Layout Design of the 3000V TSOX-MPS Rectifier

Two mask sets are developed for the TSOX-MPS rectifier. Mask set#1 includes three trench rectifiers: one large (25A current rating), one medium (10A current rating) and one small (1A current rating). Mask set #2 includes 18 trench rectifiers with different geometry. Planar devices such as the $p-i-n$ rectifier, Schottky diode rectifier and MPS rectifier are designed on the same mask for the purpose of performance comparison. Detailed information is provided in the following tables.

Table 1 Mask set #1

Device	Mesa width(μm)	Trench width (μm)	Area (/cm ²)
25A TSOX-MPS	1.5	3.0	0.5*0.5
10A TSOX-MPS	1.5	3.0	0.32*0.32
1A TSOX-MPS	1.5	3.0	0.1*0.1
10A PIN Diode	—	—	0.32*0.32

Table 2 Mask set #2

Device	Cell Geometry	Number	Comments
TSOX-MPS	Stripe	15	Mesa width from 1.0 μm to 3.0 μm , Trench from 2.0 μm to 4.0 μm
TSOX-MPS	Cylindrical	3.	With diameters of 2.0, 3.0 and 4.0 μm
MPS Rectifier	Stripe	1	P+ Imp. window width 10 μm with distance of 20 μm
PiN Diode	—	1	JTE termination
PiN Diode	—	1	FFR termination
Schottky Rectifier	—	1	—

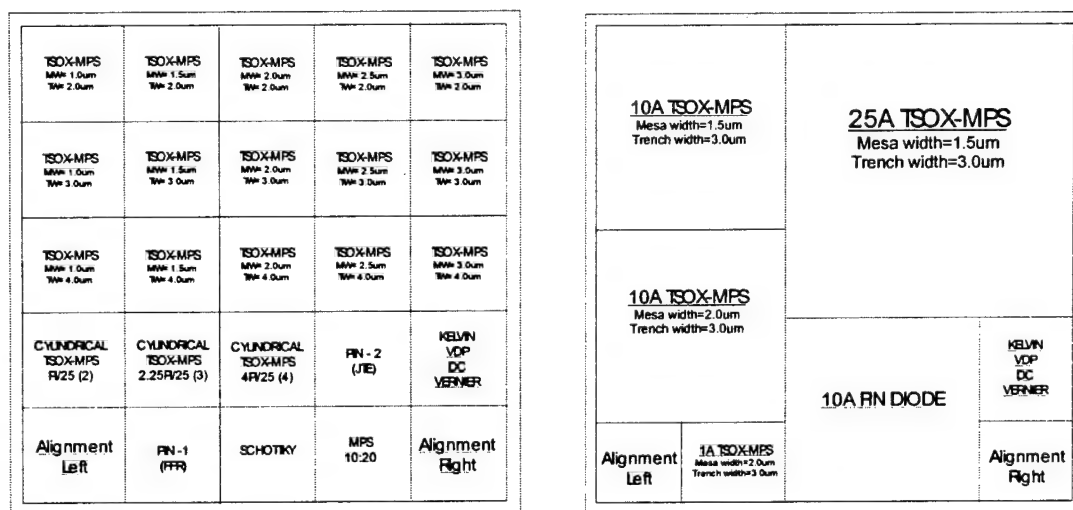


Figure 2-30. Layout of TSOX-MPS rectifiers (two sets).

The six layers that comprise the mask set are as follows:

- Field layer mask (for definition of the active area)
- P+ implantation mask
- Trench fabrication mask
- JTE implantation mask (Termination Formation)
- Contact mask

- Metal layer mask

Among them, the P+ implantation layer is exclusively used in the process of planar device fabrication. Thus, only five masks are needed for the fabrication of the trench rectifiers.

2.3.2 IGBTD

2.3.2.1 Device design

The key design parameters for the 600V IGBT and the IGBTD in our experiment are summarized in Table 3. The active area for the devices is $2.5 \times 10^{-3} \text{cm}^2$. Assuming they are operated at 100A/cm^2 , the current rating is 0.25A. The DMOS cell window was fixed at $6.5 \mu\text{m}$ for all the variations in order to facilitate comparisons. In the IGBT design, the gate lengths are varied from $5 \mu\text{m}$ to $10 \mu\text{m}$ to show the effect of JFET pinching. In the IGBTD design, similarly, the gate lengths were varied from 9 to $13 \mu\text{m}$. Notice, although the gate lengths for both the IGBT and the IGBTD are for half cells, the actual JFET pinching cannot be compared directly between the IGBT and the IGBTD due to the presence of the diverter window.

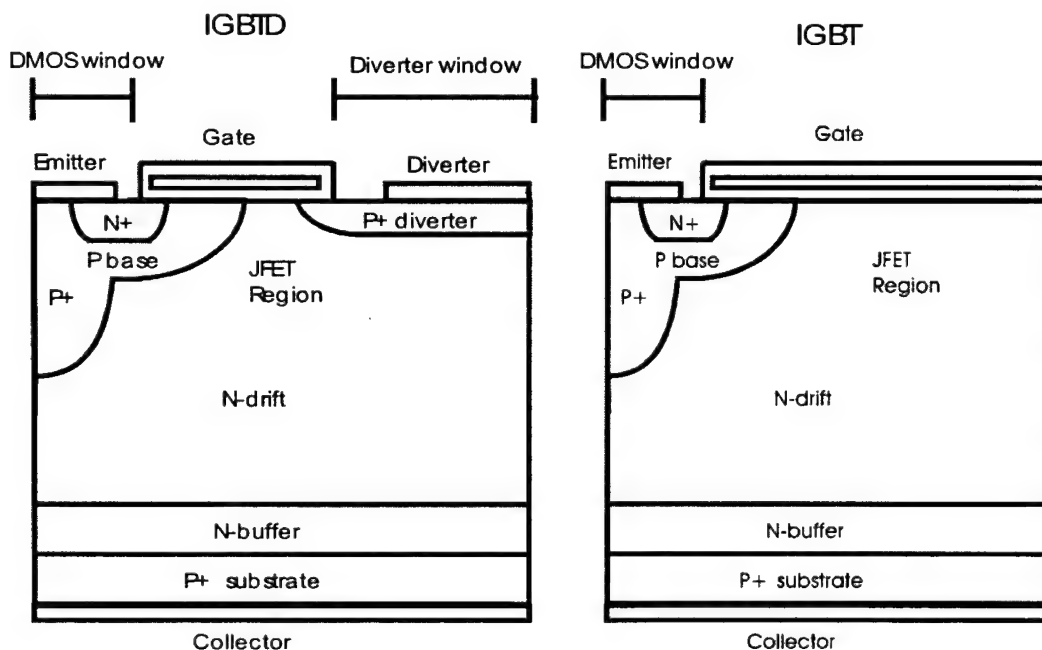


Figure 2-31. Device structures of the IGBT and the IGBTD.

Table 3 Summary of key design parameters for the stripe geometry IGBT and IGBTD

	Gate length for the half cell (μm)	DMOS window (μm)	Diverter window (μm)	Cell pitch (μm)
IGBT1	5	6.5	*****	21
IGBT2	6.5	6.5	*****	25
IGBT3	8	6.5	*****	29
IGBT4	10	6.5	*****	33
IGBTD9	9	6.5	9	40
IGBTD11	11	6.5	9	44
IGBTD13	13	6.5	9	48

The termination for the IGBT and the IGBTD were designed for a breakdown voltage of 600V. They consist of three field rings with associated field plates. The termination design is shown in Figure 2-33. This design was borrowed from a previous design of one of our group members by Z. Shen [5].

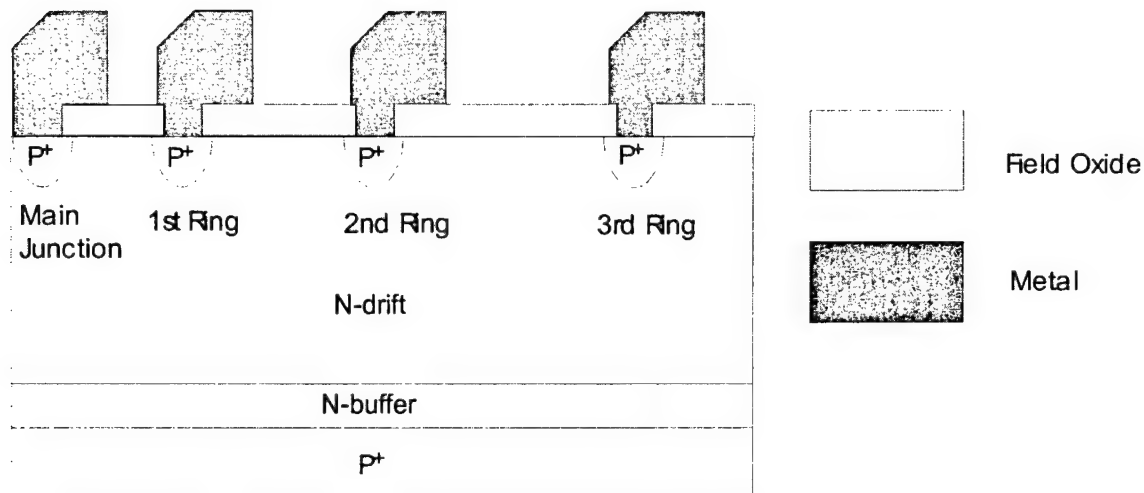


Figure 2-33. Termination structure with three field rings.

2.3.2.2 Device operation

The basic operation of the IGBT is as follows. From the circuit point of view, an IGBT is basically a cascaded BJT with MOS in a Darlington configuration (the equivalent circuit is shown in Figure 2-34). In the forward conduction, the holes injected from the collector and the electrons injected through the MOS channel create conductivity modulation in the drift region. In the forward blocking of the IGBT, the P base N drift junction is reverse-

biased and blocks the forward voltage. The IGBT retains its MOS control until it reaches the latch-up. Latch-up occurs when the P base begins to inject holes into the N^+ emitter, and the N^+ emitter injects electrons into the P base. At that point, electron current flow is no longer restricted to the MOS channel, thus making the MOS gate ineffective in controlling the current flow.

The operation of the IGBTD is similar to that of the IGBT. The equivalent circuit for the IGBTD is basically the same as that of IGBT. The difference between the IGBT and the IGBTD is that the IGBTD has an additional BJT with different β , current gain, formed by the diverter terminal and the collector. In the forward blocking mode of the IGBTD, the P diverter N drift junction is reverse-biased in addition to the P base N drift junction. One of the main differences between the IGBT and the IGBTD is that the P diverter in the IGBTD can collect some of the holes that would be collected by the P base or the P^+ . At the latching current, the hole current flowing through the P base causes the potential in the P base to rise to the point where it is forward-biased with respect to the N^+ emitter. This means that one can increase the latching current by reducing the fraction of hole current flowing through the P base. The diverter terminal shorted to the emitter is always at a lower potential than the drift region. Therefore, it can also act as a collector for holes in addition to the P base and the P^+ . In fact, due to the proximity to the MOS channel, the diverter terminal is a better collector than the P^+ . In addition, it improves further as the potential in the P base increases due to the hole current flow that increases as the P base's collection ability worsens.

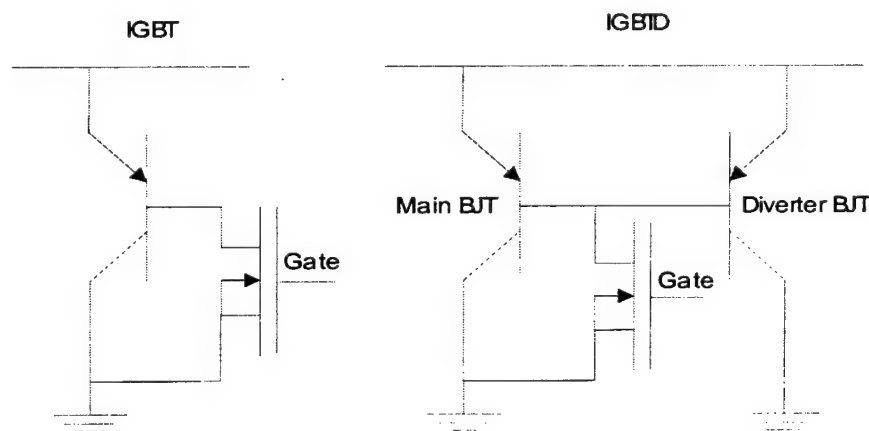


Figure 2-34. Equivalent circuits for the IGBT and the IGBTD.

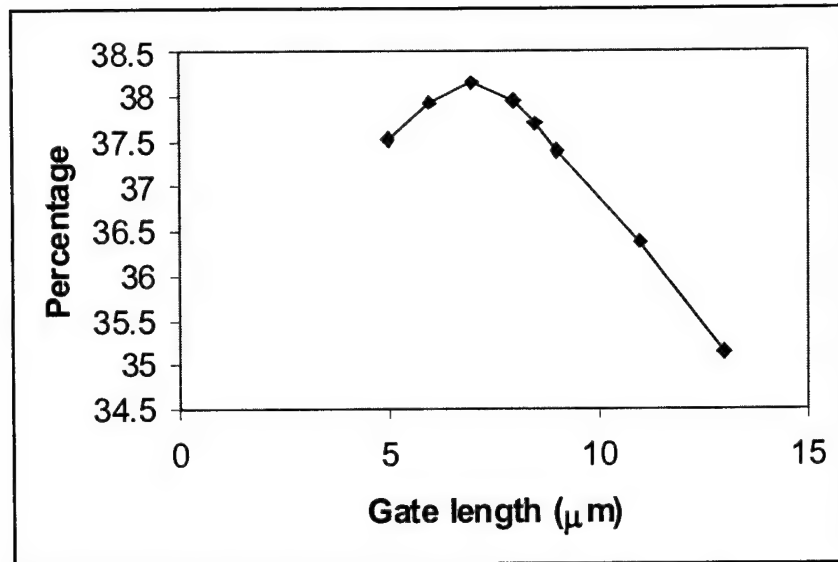


Figure 2-35. Simulated trade-off curve of the gate length vs. the percentage of the hole current collected by the diverter ($\tau_{n0}=10\tau_{p0}=1\mu\text{s}$, $L_G=9\mu\text{m}$, $J=100\text{A}/\text{cm}^2$).

Figure 2-35 shows a simulated trade-off curve comparing the gate length to the percentage of the hole current collected by the diverter. As the gate length increases, the fraction of the hole current collected by the diverter decreases. As mentioned before, the hole current and the electron current stay together in the drift region. As the diverter contact is moved away from the MOS channel, a decreasing fraction of the hole current is within the depletion region of the diverter, leading to a smaller fraction of the hole current being collected by the diverter.

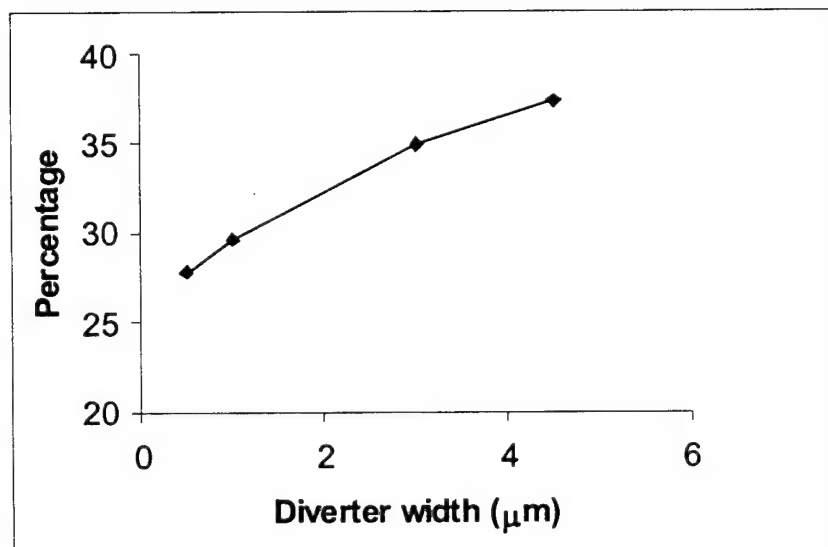


Figure 2-36. Simulated effect of the diverter width on the hole collection.

Figure 2-36 shows the effect of the diverter width on the hole collection. As the width of the diverter is increased, the diverter becomes more efficient at collecting holes. However, the increase in the hole collection is not proportional to the increase in the diverter width; there is a diminishing return. Also, additional area occupied by the diverter increases the forward voltage drop at $100\text{A}/\text{cm}^2$. Therefore, a designer has to take into account of all these factors to determine the size of the diverter terminal.

Figure 2-37 shows the trade-off curves for the gate length, L_G , and the turn-off time, t_{off} , for the IGBT and the IGBTD. As the gate length is increased, the turn-off time lengthens. As the gate length is increased, the width of the JFET region is increased. During the turn-off process, the depletion region begins to merge as the voltage blocked by the device increases. If the JFET region is narrower, the collector voltage will rise faster. This causes the collector current to decrease faster.

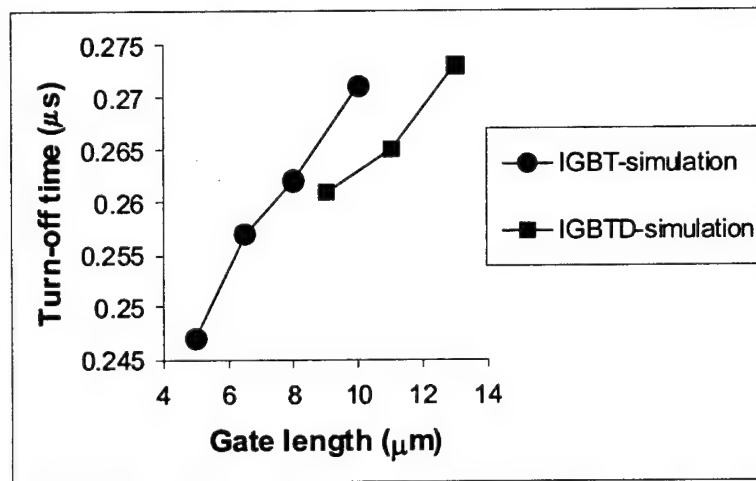


Figure 2-37. Trade-off curves for the gate length and turn-off time.

2.3.2.3 Design parameters

The drift region of the simulated 600V IGBTD structures has a doping concentration of $1 \times 10^{14} \text{ cm}^{-3}$ and a thickness of $60 \mu\text{m}$, and the buffer layer has a doping concentration of $1 \times 10^{17} \text{ cm}^{-3}$ and a thickness of $15 \mu\text{m}$. These values are chosen according to the wafers used for the fabrication. The P-base has a junction depth of $4 \mu\text{m}$ and a surface concentration of $1 \times 10^{17} \text{ cm}^{-3}$, and the N^+ emitter has a junction depth of $1 \mu\text{m}$ and a surface concentration of $1.5 \times 10^{20} \text{ cm}^{-3}$. The P^+ diverter has a junction depth of $1 \mu\text{m}$ and

a surface concentration of $8 \times 10^{18} \text{ cm}^{-3}$. The thickness of MOS gate oxide is 100 nm. The deep P^+ forms the emitter short, which is used for latch-up prevention. The doping profiles are assumed to be Gaussian except for the buffer layer and the substrate. The key parameters are listed in Table 4.

Table 4 Doping profile and geometrical dimensions used in the simulation and the design of the 600V IGBTD

N^- epi thickness	60 μm
N^- epi doping	$1 \times 10^{14} \text{ cm}^{-3}$
N buffer thickness	15 μm
N buffer doping	$1 \times 10^{17} \text{ cm}^{-3}$
P^+ substrate thickness	5 μm
P^+ substrate doping	$1 \times 10^{19} \text{ cm}^{-3}$
P -base junction depth	4 μm
P -base doping	$1 \times 10^{17} \text{ cm}^{-3}$
P^+ junction depth	6 μm
P^+ doping	$5 \times 10^{19} \text{ cm}^{-3}$
N^+ emitter junction depth	1 μm
N^+ emitter doping	$1.5 \times 10^{20} \text{ cm}^{-3}$
JFET implant junction depth	6 μm
JFET implant doping	$5 \times 10^{15} \text{ cm}^{-3}$
P^+ diverter junction depth	1 μm
P^+ diverter doping	$8 \times 10^{18} \text{ cm}^{-3}$

2.3.3 IGBT/BRT

Another important feature of the IGBT/BRT is the current saturation capability present in the IGBT mode. The current saturation capability provides a FBSOA and short circuit protection. But in the IGBT operation mode, the FBSOA is not as large as that for the IGBT because of the higher shunting resistance for the hole current. The shunt resistance consists of the P-base resistance (R_B) under the N^+ emitter region and P-MOSFET channel resistance (R_M) under the BRT gate. Reduced shunting resistance results in a higher current density at which the device could be held in IGBT mode so that a larger FBSOA could be achieved. The doping concentration of the P-base, the floating emitter length, the BRT gate length and the negative voltage applied on the BRT gate all play important roles in determining the maximum current density at which the device could be

held in the IGBT mode. The effects of these parameters on the maximum gate controllable current density are studied here in detail.

The effect of the floating emitter length, BRT gate length and the doping concentration of the P-base on maximum gate controllable current density in the IGBT mode are studied with two-dimensional numerical simulations. Figure 2-38 shows the forward I-V characteristics for different floating emitter lengths. As we can see, the maximum gate controllable current density decreases with an increase in the floating emitter length. That is because the holes injected from the P+ substrate need to travel a longer distance before they can reach the P+ diverter, resulting in a higher voltage drop along the current path. Thus, the junction between the N+ emitter and the P base will be forward-biased at a lower current density. The forward-biasing of this junction will initiate the regenerative action of the thyristor. So, by decreasing the floating emitter length, a higher maximum gate controllable current density can be achieved. This will lead to a small increase in forward voltage drop since the effective area for the thyristor is reduced. Figure 2-39 shows the forward I-V characteristics for different BRT gate lengths. The maximum gate controllable current density also decreases with an increase in the BRT gate length. The reason for this is the same as before: when there is a longer path for the hole current, it will lead to the earlier forward biasing of the N+ emitter and P base junction, which in turn starts the regenerative action of the thyristor. A shorter BRT gate length is desirable for achieving a higher maximum gate controllable current density in the IGBT mode. But there is a lower limit for the BRT gate length in order to prevent the pinch-off. Figure 2-40 shows forward I-V characteristics for different P-base doping concentrations. A high P base doping concentration leads to a less resistive path for the hole current, which results in a higher maximum gate controllable current density. On the other hand, in order to more easily initiate the regenerative action of the thyristor during turn-on, the P base doping concentration cannot be too high. Based on this, the doping concentration for the P base is selected as $8 \times 10^{16}/\text{cm}^2$.

Figure 2-41 shows the simulated FBSOA. At lower voltages, the maximum gate controllable current limits the FBSOA; at higher voltages, the avalanche breakdown

voltage limits it. Increasing the maximum gate controllable current is an efficient way to improve the FBSOA of an IGBT/BRT.

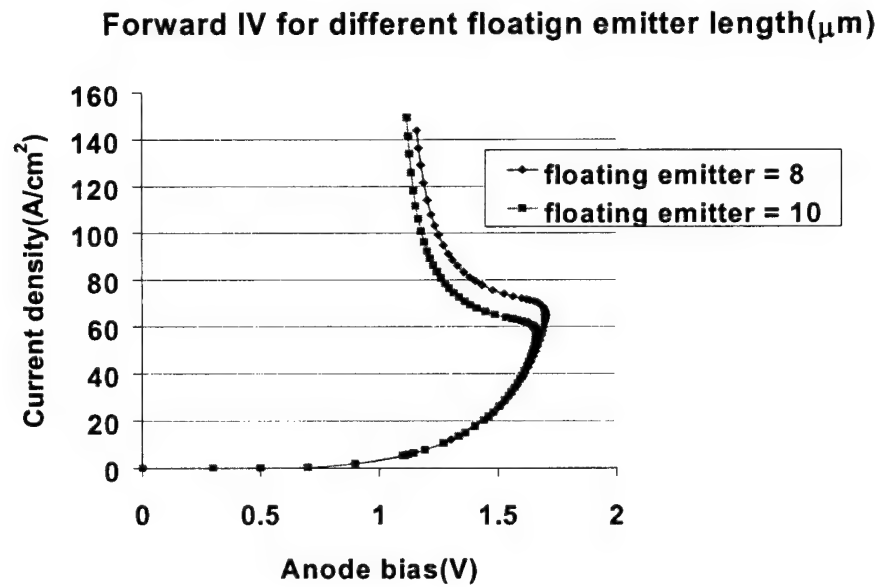


Figure 2-38. Simulated forward characteristics for different floating emitter length in the 600V IGBT/BRT.

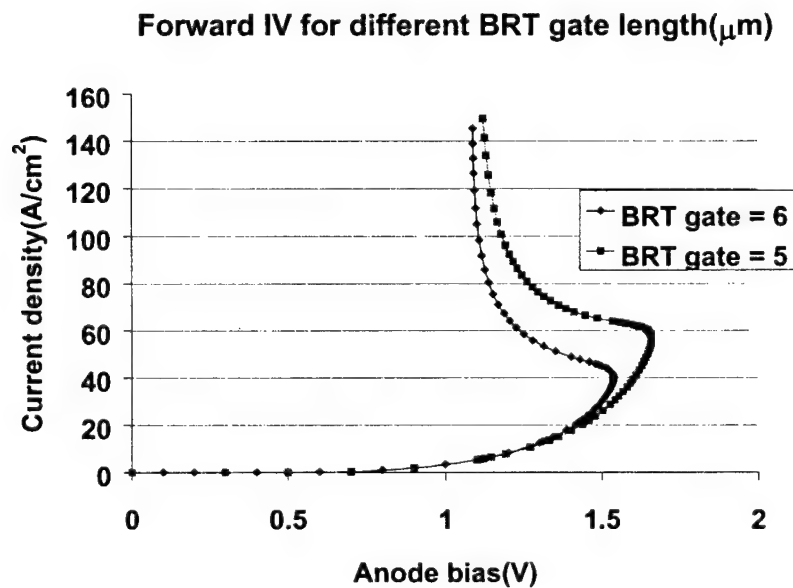


Figure 2-39. Simulated forward characteristics for different BRT gate lengths in the 600V IGBT/BRT.

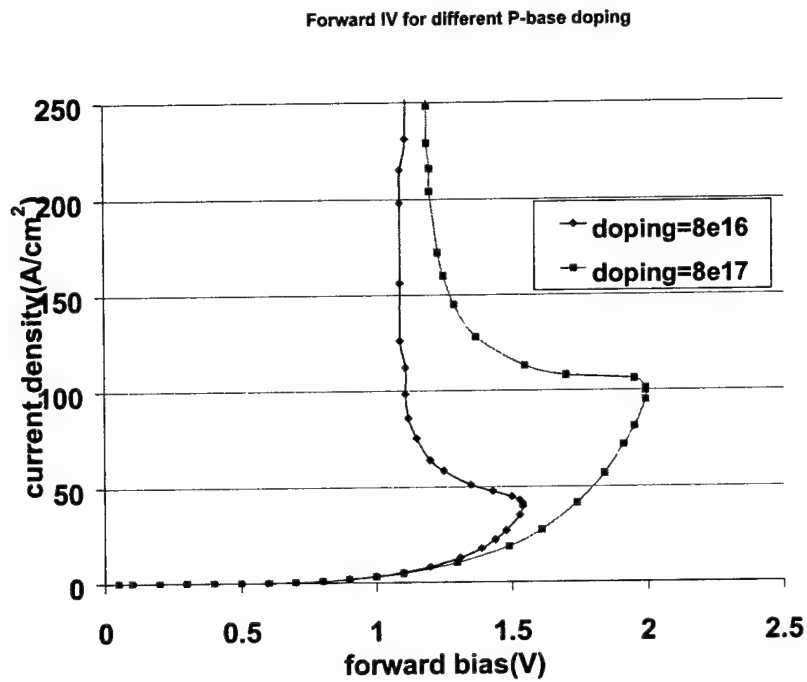


Figure 2-40. Simulated forward characteristics for different P base doping in the 600V IGBT/BRT.

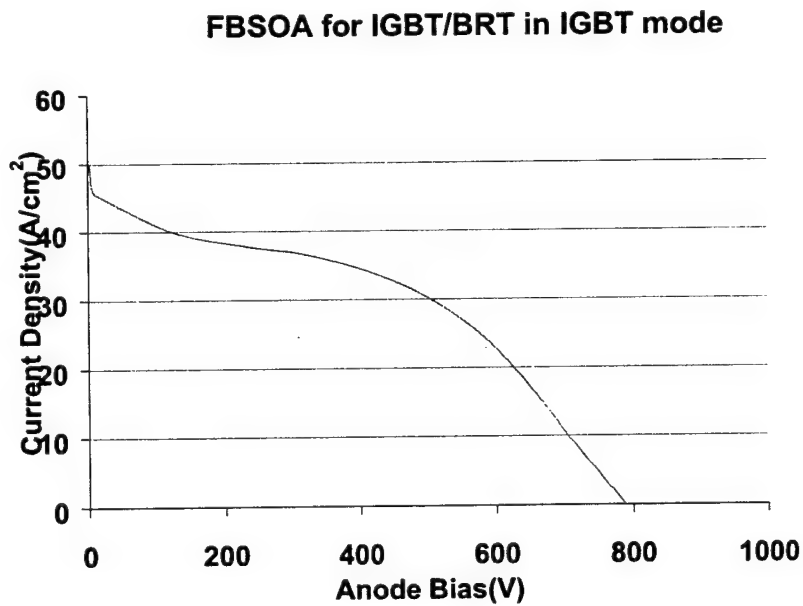


Figure 2-41. Simulated FBSOA for the IGBT/BRT in the IGBT mode.

2.3.4 Scaled-up ALL-IGBT

2.3.4.1 Device design

The scaled-up device has an active area of 0.25cm^2 . This should give a current rating of 25A if it is operated at $100\text{A}/\text{cm}^2$. The atomic lattice layout (ALL) is shown in Figure 2-42. The top view shows a circular gate with connectors extending in four directions. In actual layout, there will be identical cells arranged in square array. Figure 2-43 shows the floorplan for the big device mask. In this mask, there is one scaled-up ALL-IGBT design.

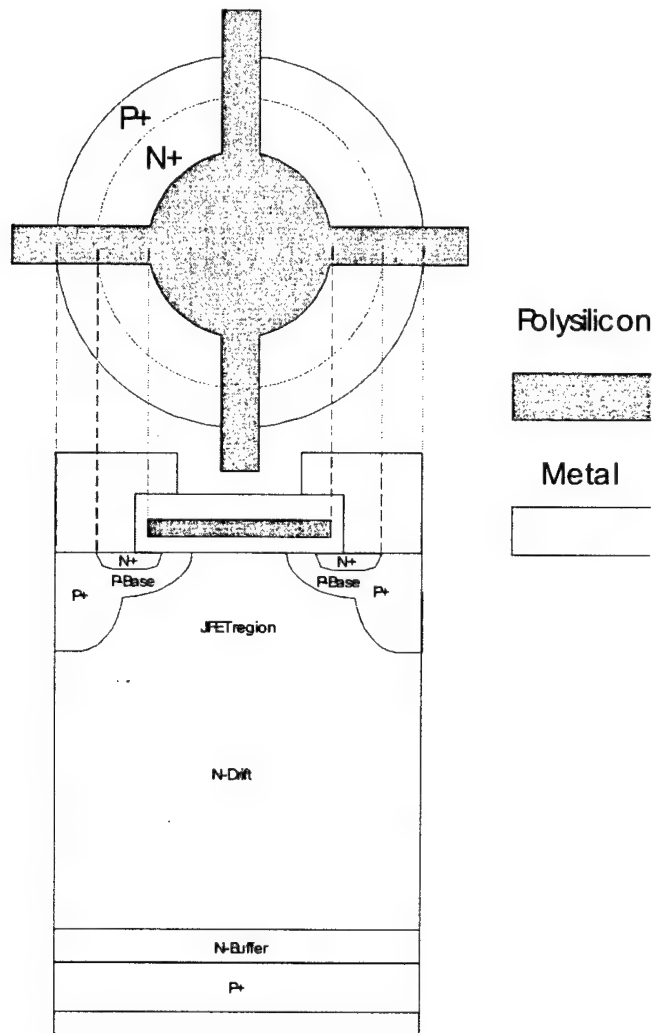


Figure 2-42. The atomic lattice layout IGBT.

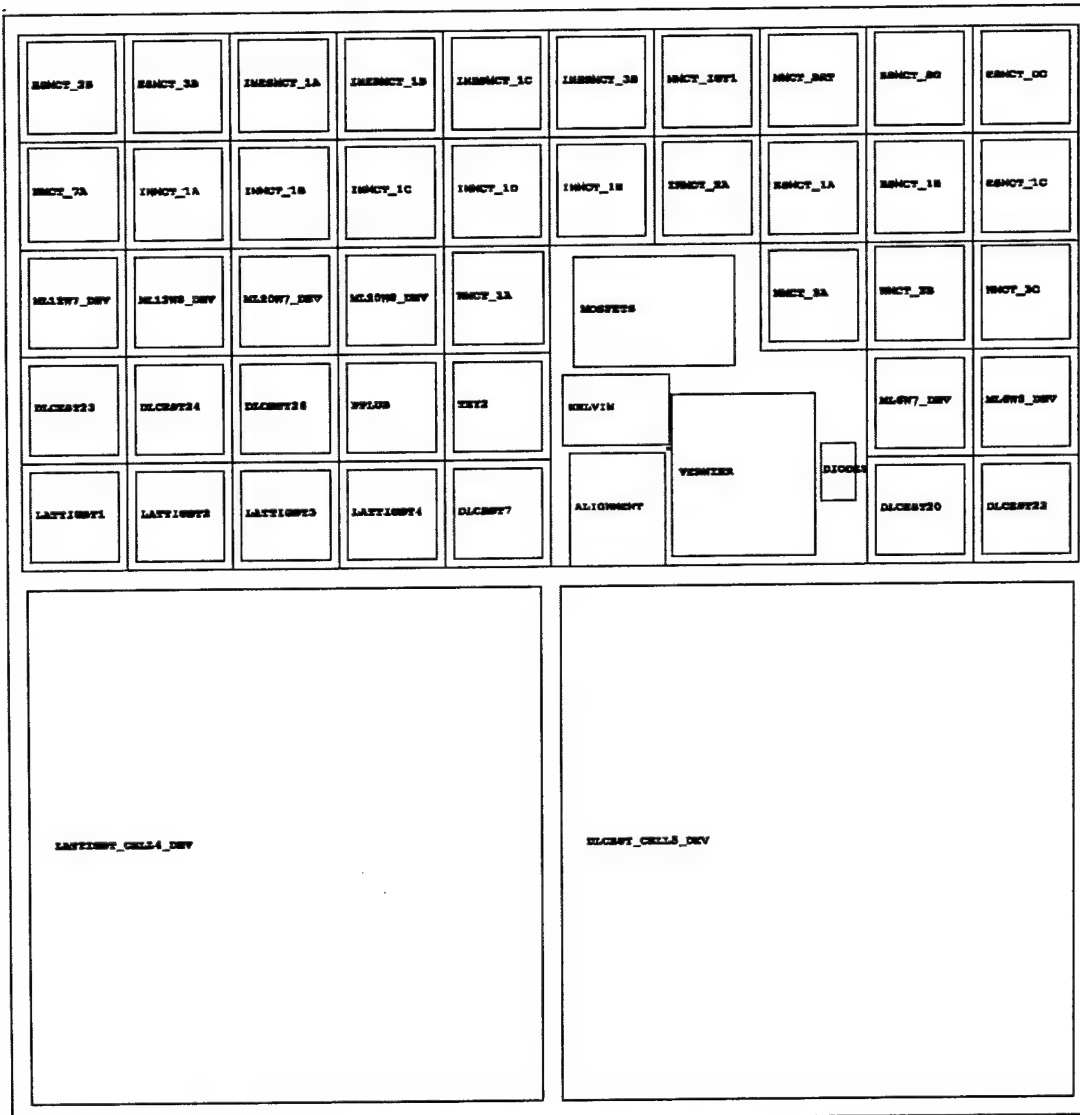


Figure 2-43. Floorplan for the big device mask.

2.3.4.2 Device operation

An ALL-IGBT is basically a cylindrically rotated IGBT design. The main motivation behind this design is to improve FBSOA. In this design, hole current in the P base region spreads out radically so that the potential in the P-base region does not build up as much as it does in a stripe design. This concept has been demonstrated in both simulation and experiments. Our goal in this project was to scale up the current rating by increasing the device area. One of the key issues in this design is reducing JFET resistance. Compared to a stripe geometry with the same gate length and JFET width, the ALL design experiences a lot more pinching due to the 2-D effect.

2.4 PROCESS STEPS

2.4.1 Prospective Process Steps for TSOX-MPS Rectifier

The key process steps used for the fabrication of the TSOX MPS rectifier are highlighted as follows:

1. Field oxidation
2. Active area patterning (Field mask)
3. Trench etching (Trench mask)
4. Oxide spacer formation
5. Polysilicon deposition, doping and planarization
6. JTE termination patterning (JTE mask)
7. Boron implantation
6. Interlevel oxide deposition
7. Contact hole patterning (Contact mask)
8. Metal deposition and patterning (Metal mask)

Table 5 Wafer specifications for the 3000V TSOX-MPS rectifier

Type	N/N+	Orient	<111>
Diameter	125mm	Resistivity	212.5- 287.5 Ω ·cm
Flat	1 Major	Thickness	390-410 μ m

The starting wafer is n^- type <111> silicon. Because of the high voltage blocking capability, the devices are fabricated directly on the substrate. The doping and thickness of the substrate are determined by the blocking voltage requirements of the device. The first step in the process sequence is the growth of the field oxide. This is done by wet oxidation at 1000°C for seven hours to give an oxide thickness of 1.3 μ m. The wafers are then patterned to define the active area. (The GCA stepper is used for exposure.) This pattern is transferred to the oxide layer by reactive ion etching in the HEXODE plasma etch tool. CHF_3/O_2 plasma is used for the oxide etching. The dry etching technique is used to minimize the undercutting that would occur with wet etching.

The formation of the trench structure is divided into the following steps:

1. Trench cell patterning and etching
2. Thermal growth of the oxide sidewall
3. Etching the bottom oxide
4. Polysilicon deposition
5. P+ implantation
6. Polysilicon deposition
7. Polysilicon planarization

To fill up the trench, polysilicon deposition is carried out in two separated steps with the implantation in between. This is done to make a uniform doping profile.

2.4.2 Process steps of IGBT, IGBTD and IGBT/BRT

The following is the overview of the process flow. First, the field oxide is grown to 1.2 μ m. Then, POCl₃ doping is done at 950 °C. In order to get rid of the PSG layer, the field oxide is deglazed. LPCVD nitride is deposited at 800 °C on both sides. Then, the nitride on top of the field oxide is etched off with RIE. Patterning of field oxide and subsequent etching is done to define the active region. The JFET is implanted with phosphorus to reduce the JFET pinching resistance. A 100nm gate oxide is grown with dry oxidation at 1000 °C. 800nm of LPCVD polysilicon is deposited on top of the gate oxide. 150nm of PECVD oxide is deposited on top of the polysilicon as a mask layer for polysilicon etching. The gate is patterned and etched down to a silicon substrate. The P⁺ implant is made. Subsequently, the P⁺ drive-in is done at 1100 °C for an appropriate time. The P Base and the P Well are patterned and implanted. Another drive-in is done at 1100 °C to achieve the junction depth of 3.5 μ m. The N⁺ and shallow N⁺ are patterned and implanted. The channel stop N⁺ is patterned and the field oxide is etched down to bare silicon. The channel stop N⁺ implant is done and then annealed at 900 °C. One 1 μ m of PECVD oxide is deposited as an inter-level dielectric. The contact is patterned and etched. Three μ m of aluminum is sputtered as the front metal. The front metal layer is patterned and etched by RIE. Sintering is done at 450 °C for 30 minutes. The backside of the wafers is lapped such that they are pared down to a thickness of 15 mils. Backside

implant of boron is done to improve ohmic contact. Finally the backside metal is sintered at 400 °C. The summary of key process parameters is in Table 6.

Table 6 The process flow with key process parameters

Process	Parameters
Grow field oxide	1.2 μm , 1000 °C, wet
Strip backside nitride	CHF_3 , O_2
POCl_3 doping for gettering	950 °C
Deglazing	BOE
Deposit LPCVD nitride	120nm, 800 °C
Etch front nitride	
Pattern active area	
Etch field oxide	
Pattern and JFET implant	Phosphorus, 100keV, $1\text{e}12\text{cm}^{-2}$
Grow gate oxide	100nm, 1000 °C, dry
Deposit polysilicon	800nm, 580 °C
POCl_3 doping	850 °C
Deposit PECVD oxide	150nm, 390 °C
Pattern gate	
Etch oxide	
Etch polysilicon	Cl_2 , BCl_3
Pattern and P^+ implant	Boron, 60keV, $1\text{e}16\text{cm}^{-2}$
Drive-in/anneal	1100 °C
Pattern and P base implant	Boron, 60keV, $1.5\text{e}14\text{cm}^{-2}$
Pattern and P well implant	Boron, 60keV, $1.5\text{e}13\text{cm}^{-2}$
Drive-in/anneal	1100 °C
Pattern and P diverter implant	Boron, 60keV, $5\text{e}15\text{cm}^{-2}$
Pattern and N^+ implant	Phosphorus, 150keV, $5\text{e}15\text{cm}^{-2}$
Pattern and shallow N^+ implant	Arsenic, 60keV, $5\text{e}15\text{cm}^{-2}$
Pattern channel Stop N^+	
Etch field oxide	CHF_3 , O_2
Channel stop N^+ implant	Phosphorus, 60keV, $5\text{e}15\text{cm}^{-2}$
Drive-in/anneal	900 °C
Deposit TEOS oxide	1 μm , 390 °C
Densify TEOS oxide	N_2 , 900 °C
Pattern contact	
Etch oxide	
Sputter aluminum	3 μm
Pattern metal	
Etch metal	Cl_2 , BCl_3
Sinter	450 °C
Backside lapping	15 mils remaining
Backside implant	Boron, 30keV, $1\text{e}16\text{cm}^{-2}$
Sputter backside metal	
Sinter backside metal	400 °C

2.5 Experimental Results

2.5.1 IGBTD

2.5.1.1 Forward conduction

Forward I-V characteristics were measured for the IGBTD and compared to those of the IGBT. Figure 2-44 shows typical I-V characteristics of the IGBT measured with the Tektronix 370A programmable curve tracer. The gate voltages used are from 5 to 25V, in 2V increments. The threshold voltage ranges from 3 to 7V, which was defined as the gate voltage at which the collector current is $1\mu\text{A}$ when the collector to emitter voltage is 10V. Figure 2-45 shows typical I-V characteristics of the IGBTD, which is basically similar to that of the IGBT. The on-resistance of the IGBTD is slightly higher than that of the IGBT. The specific on-resistance for the IGBT and the IGBTD are approximately $5\text{ m}\Omega\text{cm}^2$. Figure 2-46 shows the forward I-V characteristics of the IGBT and the IGBTD in a log scale. The IGBT has a slightly lower voltage drop at 100A/cm^2 than the IGBTD. The gate voltage used is 25V and the devices selected are the IGBT4 and the IGBTD13.

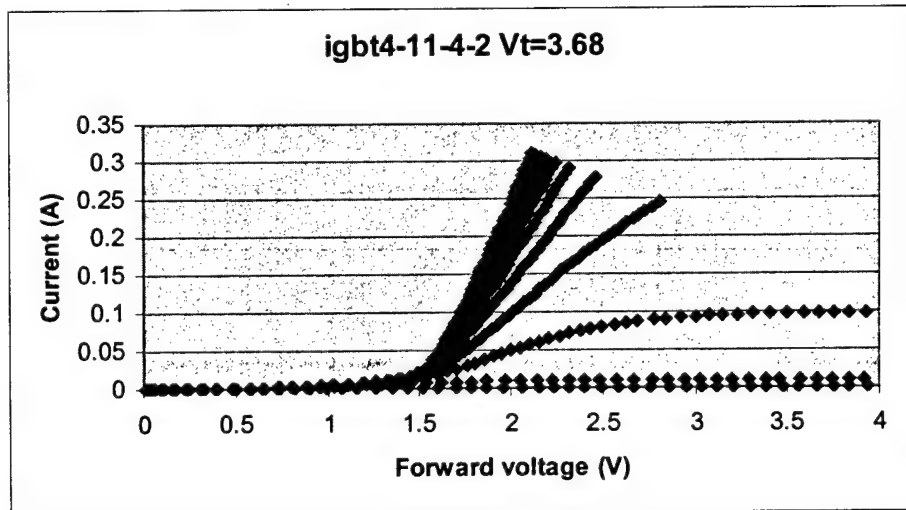


Figure 2-44. Forward I-V of IGBT.

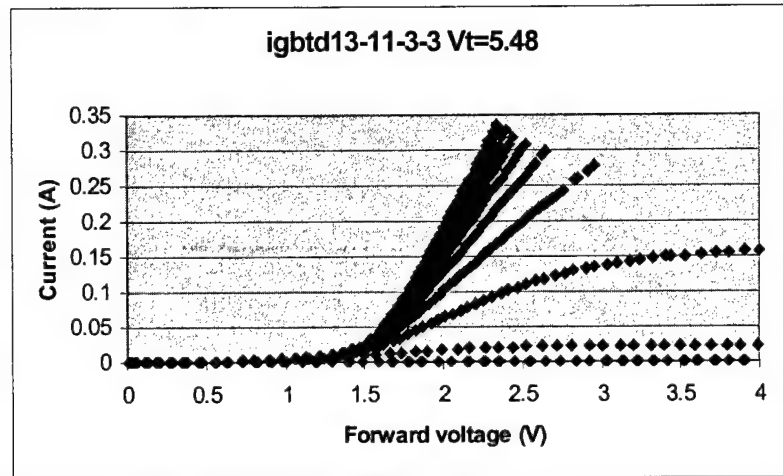


Figure 2-45. Forward I-V of IGBTD.

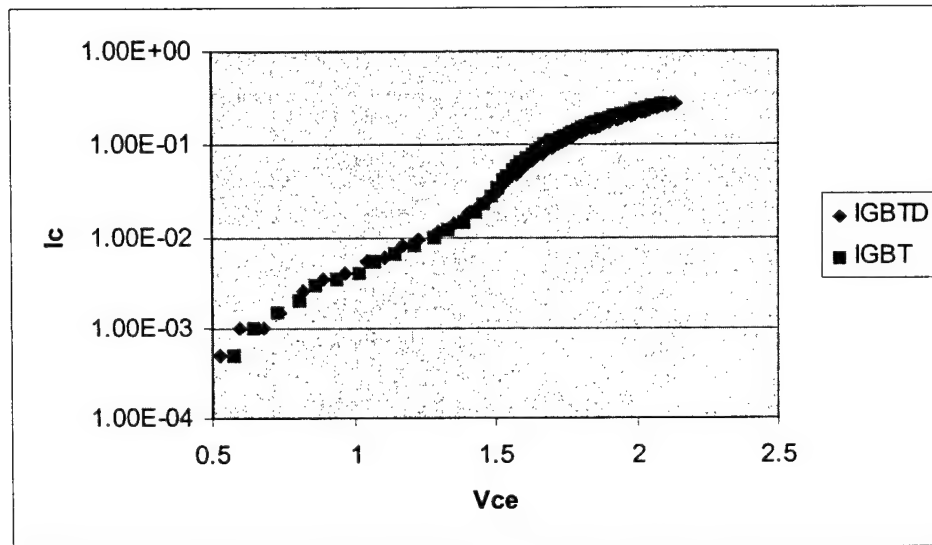


Figure 2-46. Forward I-V characteristics of the IGBT and the IGBTD in a log scale.

Figure 2-47 shows the dependence of the polysilicon gate length on the forward voltage drop at $100\text{A}/\text{cm}^2$ for the IGBT. In the case of the IGBT, the forward voltage drop increases dramatically as the gate length for the half-cell drops below $8\mu\text{m}$. This is due to pinching off of the JFET region. It appears that from 8 to $10\mu\text{m}$ there is no significant improvement in the forward drop as the gate length changes. Although the reduced JFET resistance lowers the forward voltage drop at $100\text{A}/\text{cm}^2$, the increased cell size reduces the channel density for larger gate length. In fact, it is expected that as the gate length increases further, the forward voltage drop will eventually increase, thus the optimal gate length should exist at some finite gate length. In the case of the IGBTD, there is a steady

improvement as the gate length changes from 9 to 13 μm . This indicates that there is still more forward voltage drop to gain by increasing the gate length for the IGBTD.

The width of the JFET region can be calculated by subtracting the lateral diffusion from the gate length. For example, the IGBT3 has 8 μm gate length for the half-cell. Since the P base diffusion is about 3 μm , the JFET width for that variation is 7 μm for the half-cell. On the other hand, IGBTD9 has 9 μm gate length for the half-cell. Since the IGBTD has a lateral diffusion from the diverter as well as from the P base, it has a smaller JFET width than an IGBT with the same gate length. In our process, the diverter diffusion was designed to be 1 μm , and the JFET width comes out to be 7 μm , which is same as that of the IGBT3.

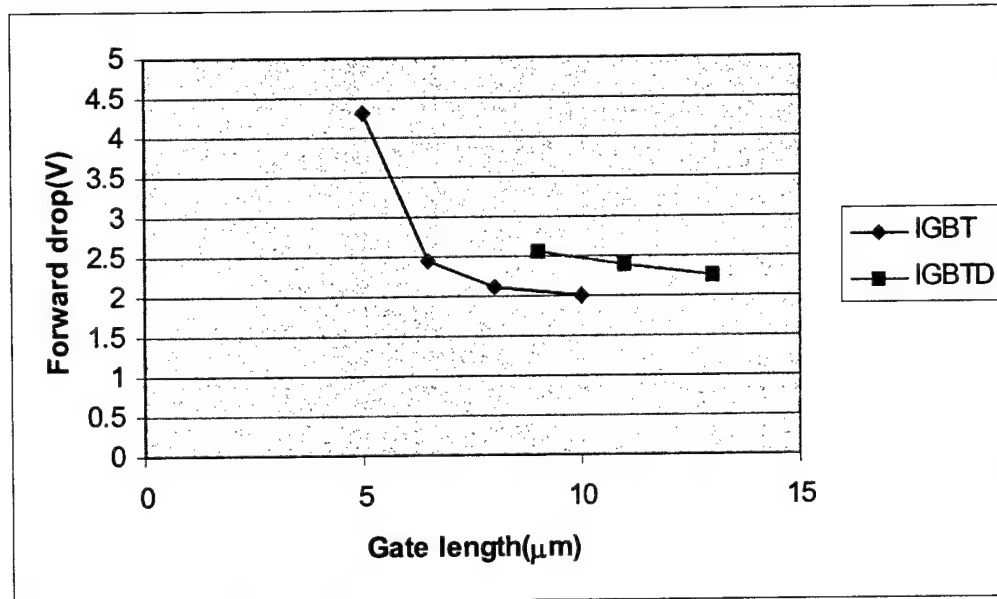


Figure 2-47. Effect of gate length on the forward voltage drop.

2.5.1.2 Forward blocking

The best breakdown voltage measurement is shown in Figure 2-48. The breakdown voltage is measured to be about 550V, which is close to the design goal of 600V. The leakage current at a collector voltage of 200V was measured for the IGBT and IGBTD. The leakage current measurements are summarized in Figure 2-49. A total of 26 devices were used for the leakage current and the breakdown voltage measurements. As shown in Figure 2-49, most of the devices measured have leakage currents less than 10 μA .

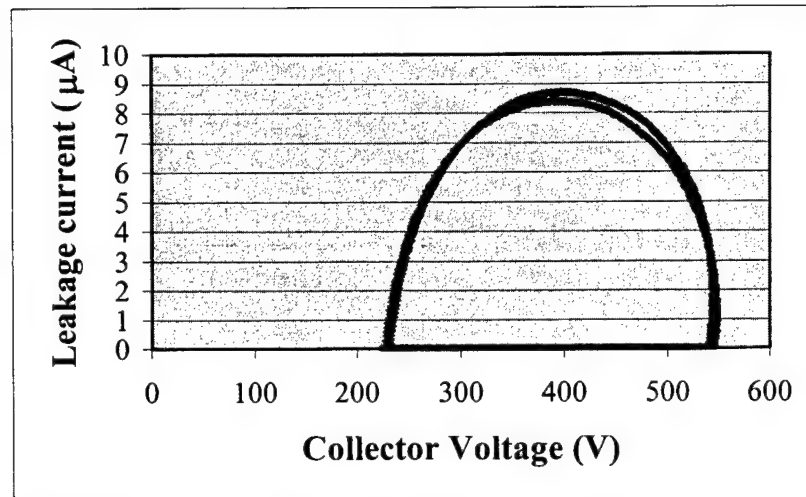


Figure 2-48. The best measured breakdown voltage of the IGBT and the IGBTD.

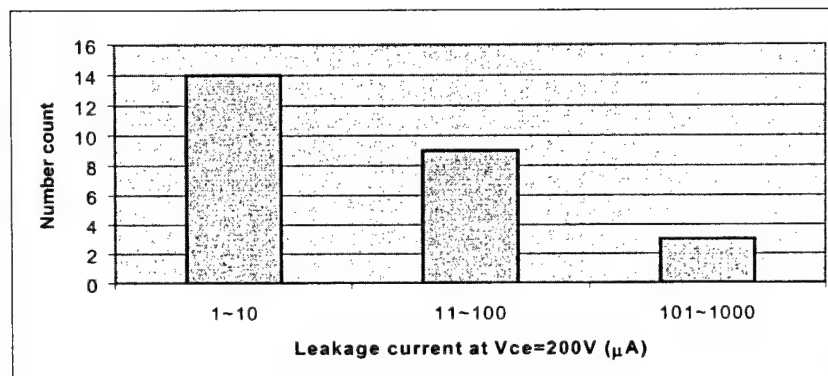


Figure 2-49. Leakage current measurements for the IGBT and the IGBTD.

2.5.1.3 Switching

Figure 2-50 and Figure 2-51 show the turn-off transient of the IGBT and IGBTD.

A turn-off time t_{off} is measured from the time the gate signal begins to drop to the time the collector current is 10% of its on-state value. IGBT turn-off waveform can be divided into two regions.

The first region comes about due to the steady decrease in the MOS current as the gate voltage drops off. The second region is where stored holes show an exponential decay due to recombination. This second region can be divided into two sub-regions: the high-level and the low-level injection regions. Since the device was in high injection region in the on-state, it remains there until the current level decreases enough that it enters the

low-level injection region. From the turn-off curve, one can extract the high-level and the low-level lifetime by examining the slope of exponential tail. Figure 2-52 shows the turn-off waveform in a log scale. As seen in Figure 2-52, τ_{p0} and τ_{n0} are calculated to be $0.10\mu\text{s}$ and $1.0\mu\text{s}$ respectively from the slope of the turn-off tail.

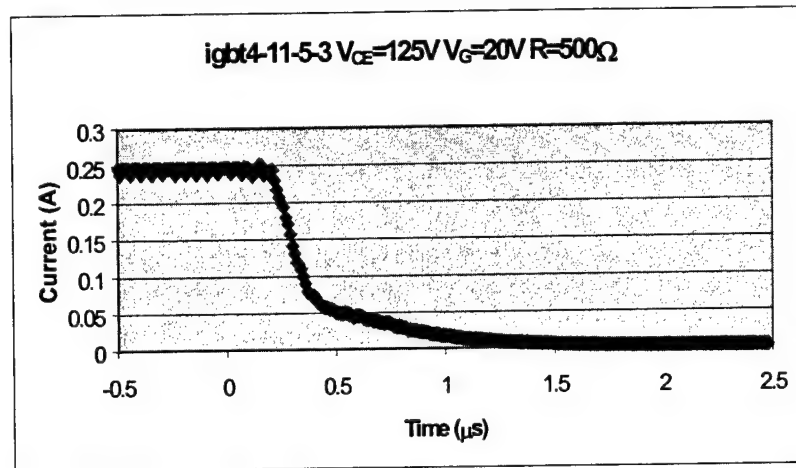


Figure 2-50. Turn-off waveform of IGBT.

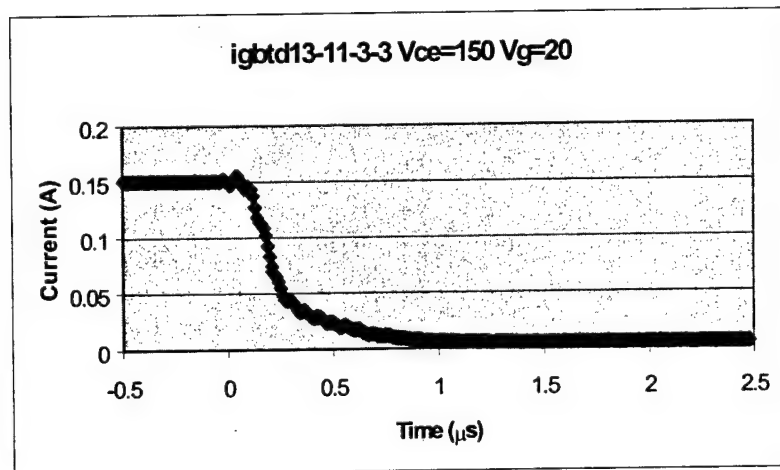


Figure 2-51. Turn-off waveform of IGBT.

There is a trade-off between the forward voltage drop and the turn-off time. The turn-off time can be reduced if the minority carrier lifetime is short. However, that tends to reduce the gain of the BJT by reducing the base transport factor. Therefore, in order to compare different device types, it might be useful to compare the trade-off plots of V_{CE} vs. t_{off} . The trade-off plots of the IGBT and the IGBT are shown in Figure 2-53. The IGBT, the

which has the smallest JFET width, has the highest forward drop but the shortest turn-off time among the IGBTD variations. The IGBTD13, which has the largest JFET width, has the lowest forward drop and the longest turn-off time among the IGBTD variations. A similar trend is seen in the IGBT variations. The IGBTD has a slightly better trade-off than the IGBT (Figure 2-53).

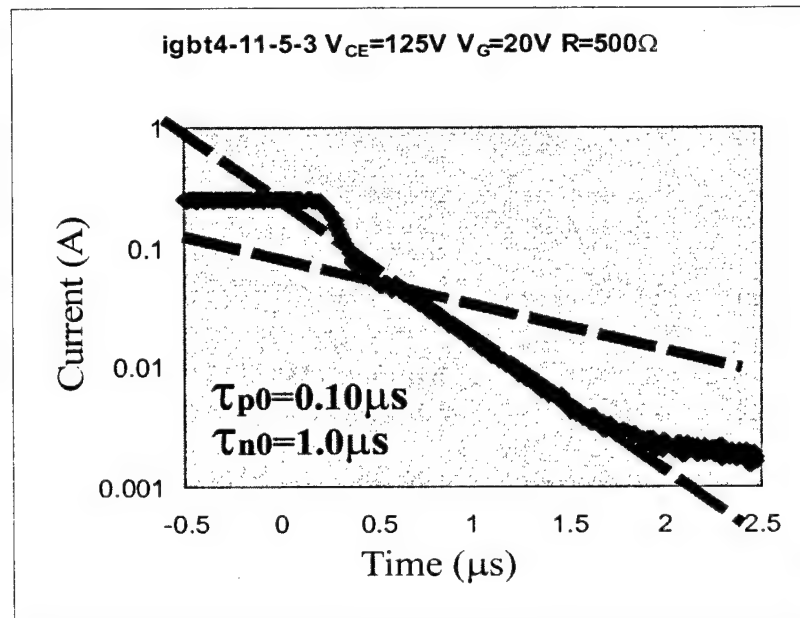


Figure 2-52. Extracted carrier lifetime from the turn-off waveform of the IGBT.

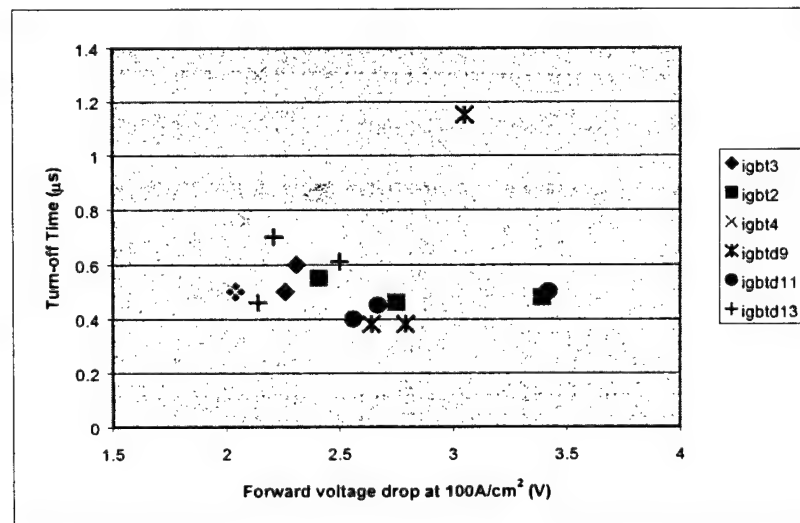


Figure 2-53. Trade-off plot between V_{CE} and t_{off} for the IGBT and the IGBTD.

2.5.2 IGBT/BRT

There are nine different design variations for the IGBT/BRTs. The key design parameters are summarized in Table 7.

Table 7 Design variations for IGBT/BRT

Device Name	IGBT Poly width(μm)	BRT Poly width(μm)	BRT window width(μm)
IGBTBRT1	12	6	10
IGBTBRT2	14	6	10
IGBTBRT3	16	6	10
IGBTBRT4	12	7	10
IGBTBRT5	14	7	10
IGBTBRT6	16	7	10
IGBTBRT7	12	8	10
IGBTBRT8	12	5	10
IGBTBRT9	12	6	20

2.5.2.1 Forward I-V Characteristics Measurement

The forward IV characteristics of the IGBT/BRT in different operation modes are measured with a curve tracer. Figure 2-54 shows the measurement results. The forward IV for an IGBT with same cell pitch is shown for comparison. The measurement results are consistent with those of the simulations. At the current density level of 50 A/cm², the forward voltage drop for the thyristor operation mode, the IGBT operation mode and the IGBT are 1.52V, 2.12V and 1.71V, respectively. The reason for the difference in the forward voltage drop is the same as was explained in the simulation results. The measured forward voltage drop is higher than in the simulation results. Also, the device exhibits a diode knee, which is due to the presence of the collector junction between the P⁺ substrate and the buffer layer. When the minority lifetime of the N buffer layer is smaller than expected, the injection of holes from the P⁺ substrate will not be very effective at the normal ideal emitter/collector junction bias. This means the conductivity modulation in the N drift region is not very efficient at the normal emitter/collector bias. So, at the same current density level, the measured forward voltage drop is higher than in the simulation. In this regime, the device can be modeled as a diode in series with a large value resistor.

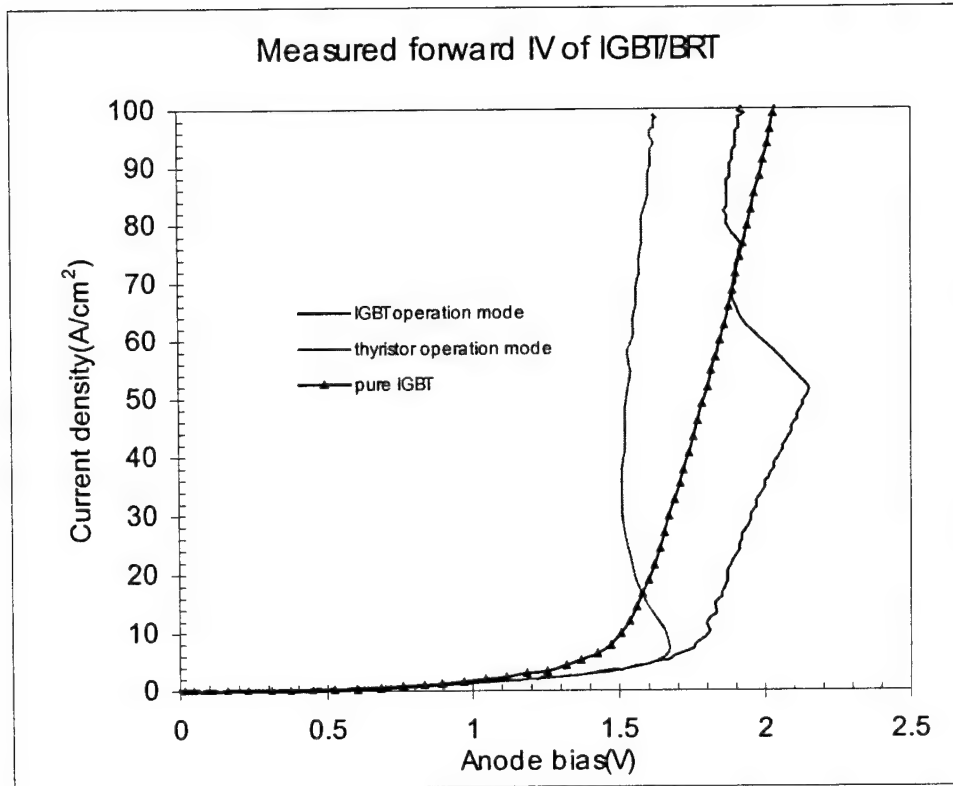


Figure 2-54. Measured forward IV characteristics for the IGBT/BRT in different operation modes and the IGBT.

As the anode bias is increased, more holes are injected from the P+ substrate into the N drift region, which will in turn result in a higher degree of conductivity modulation and reduced region resistance for the N drift region. This is the reason for the negative resistance region. Some defects at the junction between the N- buffer/P+ substrate might be another reason for the negative resistance region. If due to some defects at the junction, the N- buffer and P+ substrate are shorted together, this will also influence the injection of the holes into the N-drift region. Cutting the device into smaller dies might help to alleviate this problem, since it will reduce the possibilities of junction shorting.

2.5.2.2 Forward Blocking Measurements

Forward blocking characteristics of the IGBT/BRT were measured. The forward blocking voltage was designed to be 600V, which is the breakdown voltage of the termination design borrowed from Z. Shen [5]. However, the measured breakdown voltages are typically about 500V. Figure 2-55 shows the measured forward blocking characteristics

of the IGBT/BRT. There are a number of factors that contribute to this reduction of the breakdown voltage. First, the field oxide under the field-limiting ring was designed to be $1\mu\text{m}$. However, during the fabrication of the device, much of it was lost due to repeated photo resist ashing steps. The actual field oxide thickness is around $0.6\mu\text{m}$. This increases the curvature of the depletion region, which leads to the reduction in the forward blocking capability. Second, since no passivation layer is used for the devices, the introduction of the sodium ions reduces the breakdown field for the field oxide, thereby reducing the breakdown voltage. In addition, the N buffer/N drift interface does not have the abrupt doping profile assumed in the simulation. There are numerous high-temperature steps during the process. During these high-temperature steps, the high concentration of impurities in the N-buffer layer has many opportunities to diffuse into the lightly doped N-drift region. This effectively reduces the thickness of the N-drift region, which reduces the forward blocking voltage.

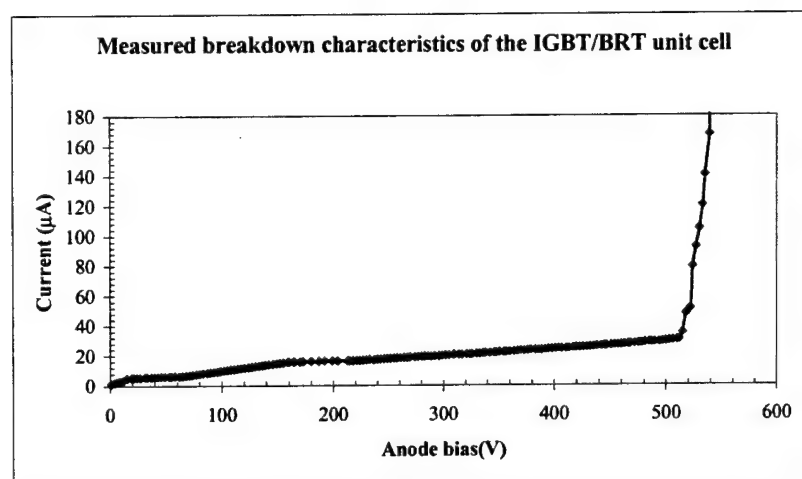


Figure 2-55. Measured blocking characteristics of the IGBT/BRT.

2.5.2.3 Switching Characteristics Measurements

The turn-off time is a very important parameter in characterizing a device. The faster a device can be turned off, the less power will be lost and less heat will be dissipated. Less power loss improves the efficiency of the circuit.

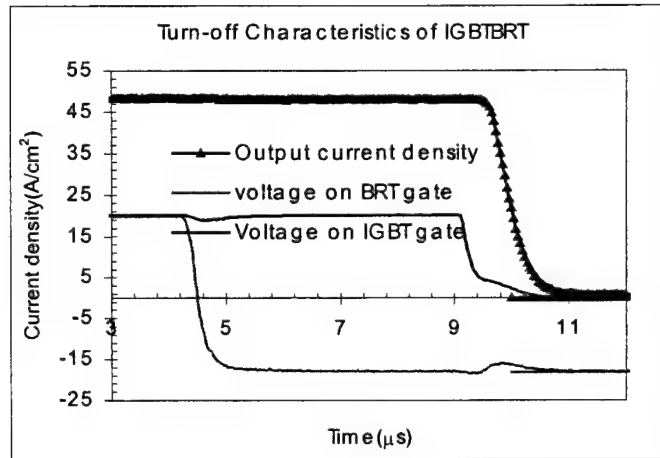


Figure 2-56. Measured turn-off characteristics of the IGBT/BRT.

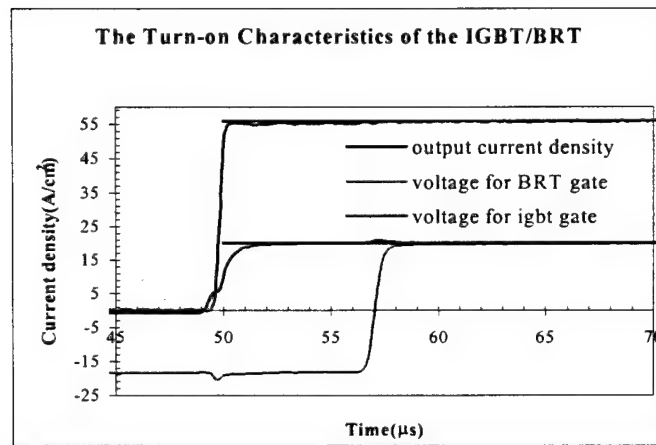


Figure 2-57. Measured turn-on characteristics of the IGBT/BRT.

When the transient behavior of the IGBT/BRT is tested, two separate gate signals with timing requirements are needed. Since the pulse generator cannot meet the specific requirements, a gate signal circuit was designed to supply the gate signal needed for the switching testing. At the initial stage, both signals have a constant positive value of 25V and time t_D . Before the device needs to be turned off, the gate signal connected to the BRT gate is switched to a negative value of -20V in 200 ns. With the negative voltage on the BRT gate, the P channel MOSFET will be turned on, which will shunt away the hole current. Then the device is switched from the thyristor operation mode to the IGBT mode, and the signal connected to the IGBT gate is reduced to zero to turn the device off in the IGBT operation mode. The delay t_D between the two gate signals could be varied to

study the effect of this factor on the mode switching. Figure 2-56 and Figure 2-57 show the switching measurement results. At certain current density level, the device can be switched between its two different operation modes and turned off in the IGBT operation mode, as designed. The current density at which the device operation modes can be switched is lower than the static case due to the large dI/dt experienced during the transient process.

The carrier lifetime can be extracted from the turn-off waveform of the IGBT. Initially, the collector current drops sharply (due to the turn-off of the N-channel), from which the electrons in the N⁺ emitter are injected into the N-drift region. Then, the stored charge decays through the recombination process. Initially, while the collector voltage has not risen significantly, the depletion region does not sweep the entire drift region. In this case, most of the carriers are stored in the drift region, so most have the high-level lifetime. When the collector voltage has risen significantly such that the entire drift region is depleted, the carriers are stored in the buffer region that is doped much higher than the drift region. In this case, the carriers have the low-level lifetime. This can be seen in the turn-off waveform if the current is shown in a log scale. There will be two different slopes for the decay, one representing the high-level lifetime in the drift region and the other representing the low-level lifetime in the buffer region. Assuming the ratio between the τ_{n0} and the τ_{p0} to be about 10, the lifetime can be extracted from the turn-off waveform. This phenomenon is not obvious for IGBT/BRT, due to the presence of the thyristor structure in parallel with the IGBT structure. Figure 2-58 shows the trade-off curves between the forward voltage drop V_F and the turn-off time t_{off} . Neither the IGBT Poly-Si nor the BRT Poly-Si regions are active during the on-state thyristor operation mode. In this mode, the majority of the collector flows through the BRT window. So when the gate Poly-Si widths are increased, the inactive region in the on-state will increase also. At the same current density level, this will lead to a higher forward voltage drop. Once the device switches to the IGBT operation mode, the BRT window region no longer conducts current. So, a large IGBT area will lead to a fast turn-off process.

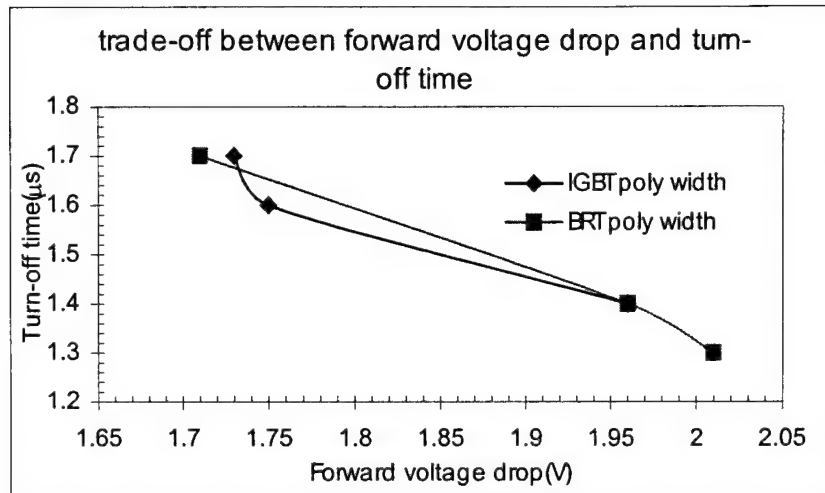


Figure 2-58. Measured trade-off between forward voltage drop and turn-off time for gate poly widths.

2.5.2.4 Maximum Gate Controllable Current Density Measurements

The effect of different device geometries and operating conditions on the maximum gate controllable current density is also studied with the measurement results. Figure 2-59 shows the effect of BRT Poly-Si width on the maximum gate controllable current density. When the BRT Poly-Si width is increased, the channel length of the P MOSFET is also increased, which means a longer hole-shunting path when the device is operated in the IGBT mode. At a lower current density, the lateral voltage along the hole current path will be high enough to forward-bias the N+ emitter/P-well junction. Figure 2-60 shows the effect of BRT gate voltage on the maximum gate controllable current density. For this same reason, a lower BRT gate voltage leads to a more resistive path for the hole current. The forward biasing of the upper junction will happen at a lower current density level. Figure 2-61 shows the effect of operating temperature on the maximum gate controllable current density. The experimental results follow the same trends as the simulation. The discrepancy of the actual maximum gate controllable current density exists because the lifetime used in the simulation is different from the actual lifetime in the N-drift region.

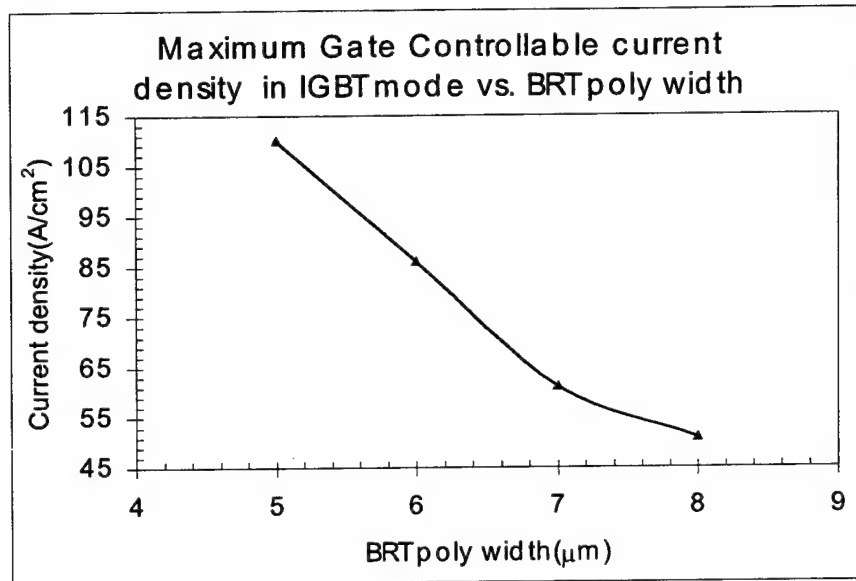


Figure 2-59. Measured effect of the BRT Poly-Si width on the maximum gate controllable current density.

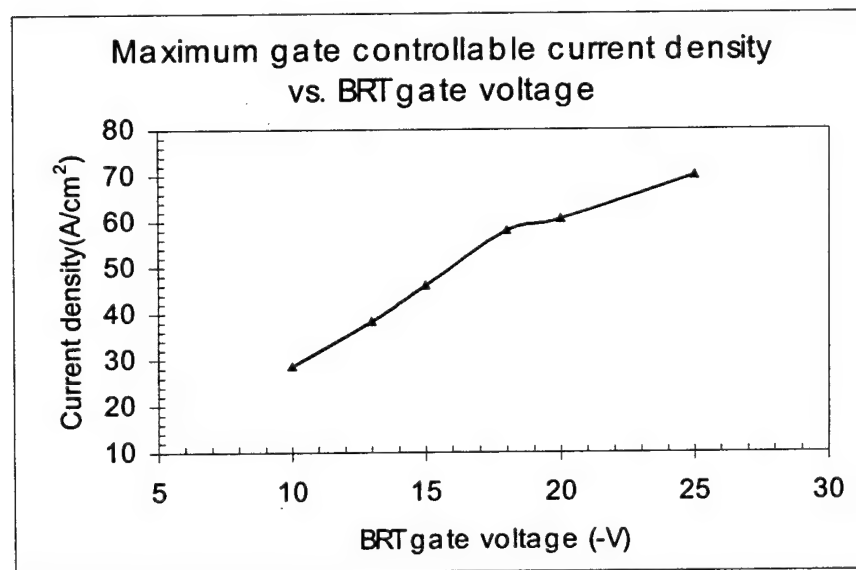


Figure 2-60. Measured effect of the BRT gate voltage on the maximum gate controllable current density.

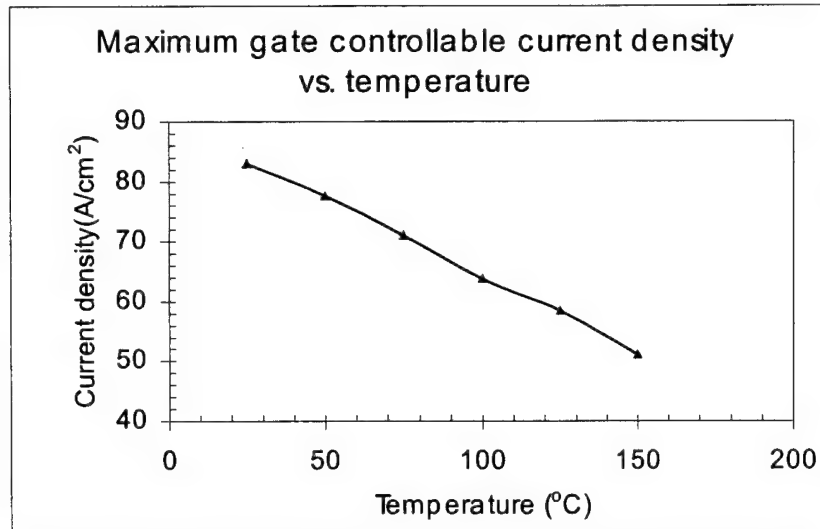


Figure 2-61. Measured effect of the operating temperature on the maximum gate controllable current density.

2.5.3 Scaled-up ALL-IGBT

A typical Forward I-V is shown in Figure 2-62. The on-resistance is approximately 0.67Ω , which corresponds to the specific on-resistance of $0.17\Omega\text{cm}^2$. This high specific on-resistance can be attributed to the JFET resistance. In our design, the radius of the polysilicon gate was $10\mu\text{m}$. It caused an excessive pinching of the JFET region. This JFET resistance contributed significantly in the total on-resistance.

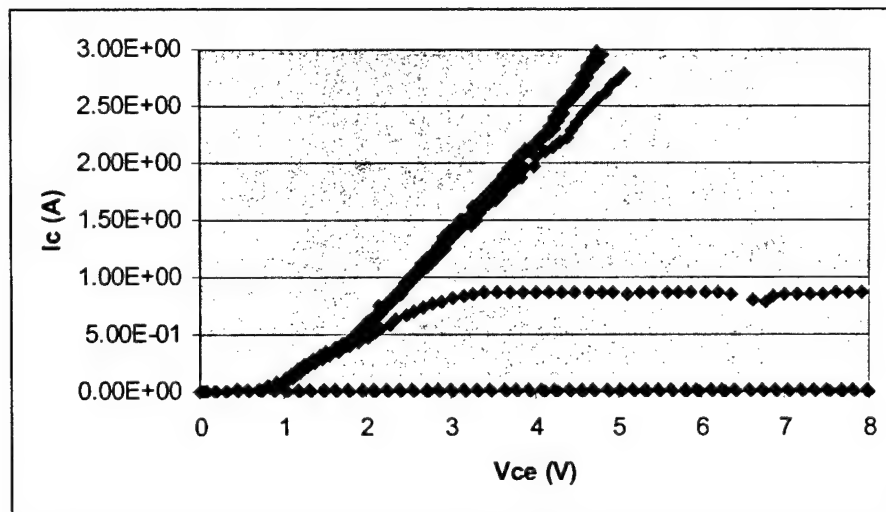


Figure 2-62. Forward I-V of the scaled-up ALL-IGBT.

2.6 References

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Chapter 3 Three-Stage Active Gate Drive and Fast Fault Current Limiting Protection for High Power IGBT PEBBs

Active gate drive and fault protection technology can be used to obtain high performance switching and fault protection characteristics in insulated-gate bipolar transistor (IGBT) power electronics building blocks (PEBBs). This chapter reports the results obtained using the integrated three-stage active turn-on and turn-off gate driver with the fast fault current limiting protection circuit. The proposed three-stage active gate drive technique is verified to be able to operate under the wide range of temperature conditions experienced by the devices. The integrated fast fault protection circuit allows the active gate drive to operate at a higher on-state gate voltage, which reduces the conduction loss. Also, due to the fault management strategy, the active drive circuit can improve the fault endurance capability of the device.

3.1 Introduction

The gate drive circuit in a power converter is critical to the performance and reliability of the power converter. Today it is possible to build mega-watt power converters using high-voltage IGBTs (HVIGBTs) [1], [2]. Limitations of the HVIGBTs available today include the following: the di/dt magnitude during switching, due to the reverse recovery characteristics of the free-wheeling diode during turn-on; and the over-voltage generated during turn-off, due to the parasitic inductance in the module and bus structure [3].

To overcome limitations of conventional gate drive (CGD) circuits that use fixed-gate resistors, several active gate drive (AGD) circuits have been proposed and widely studied [4]-[6]. By reducing the turn-on and turn-off stresses the AGDs improve the switching characteristics, which can lead to improved utilization of the IGBT in the power converter. Circuits that improve the switching performance under normal conditions can result in degraded performance under fault conditions. Traditionally, fault current limiting circuits (FCLCs) have been studied in order to improve the fault endurance capability of IGBTs [6]-[8]. An integrated approach that seeks to improve switching and fault characteristics is important in gate drive design. This research focuses on the three-

stage AGD technique and shows how it can be extended to include short circuit protection in IGBTs [9].

3.2 Three-Stage Active Gate Drive Scheme

To obtain optimized behavior for the high power IGBTs, the three-stage AGD technique is integrated with a fault current limiting circuit. Such an IGBT gate drive has the following characteristics:

- Turn-on is optimized by reducing the delay time, controlling the turn-on di/dt and the associated reverse recovery effects, lowering the tail voltage and the associated tail voltage loss, and reducing the overall turn-on time.
- Turn-off is optimized by reducing the delay time, controlling the over-voltage, reducing the turn-off loss due to improved dv/dt characteristics, and reducing the total turn-off time.
- Lower conduction loss in the IGBT is obtained by using a higher on-state gate voltage. Both the initial peak fault current and the clamped fault current can be lowered by the use of fast clamped fault protection.
- Soft turn-off is provided after over-current and short current faults to limit the peak collector voltage.

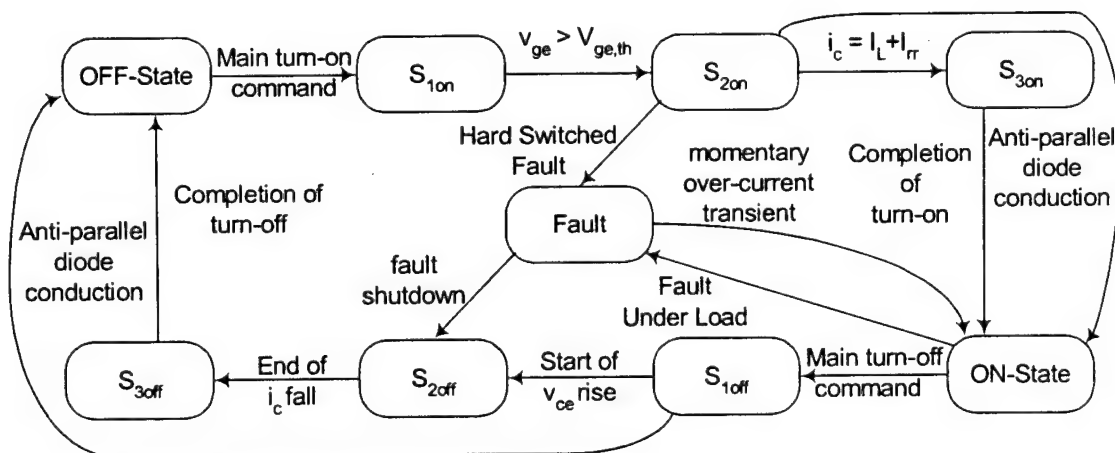


Figure 3-1. The state transition diagram of the three-stage AGD circuit.

The proposed AGD circuit uses a three-stage control technique for turn-on and turn-off. It is based on applying appropriate gate control during the different stages of the switching transient of an IGBT [10], [11]. The state transition diagram for the three-stage AGD with the protection circuit is shown in Figure 3-1. During an IGBT turn-on switching transient, stage I would correspond to the delay time, stage II to the current rise time, and stage III would correspond to the voltage fall and the time required for the gate voltage to reach the positive gate bias voltage level (V_{gg+}) from the Miller Plateau. The active gate control during the first stage is designed to minimize the delay time. The second stage controls the di/dt and dv/dt during switching. The third stage results in the IGBT rapidly reaching its final steady state. If the freewheeling diode conducts the load current during turn-on, then the current rise duration is zero. Under these conditions in the three-stage AGD, the rapid charging action of the gate in stage I up to the IGBT's gate threshold voltage is followed by stage II during which the gate is slowly charged to V_{gg+} . If the freewheeling diode conducts during the turn-off command of the IGBT, there is no rise in the collector voltage after the turn-off delay time.

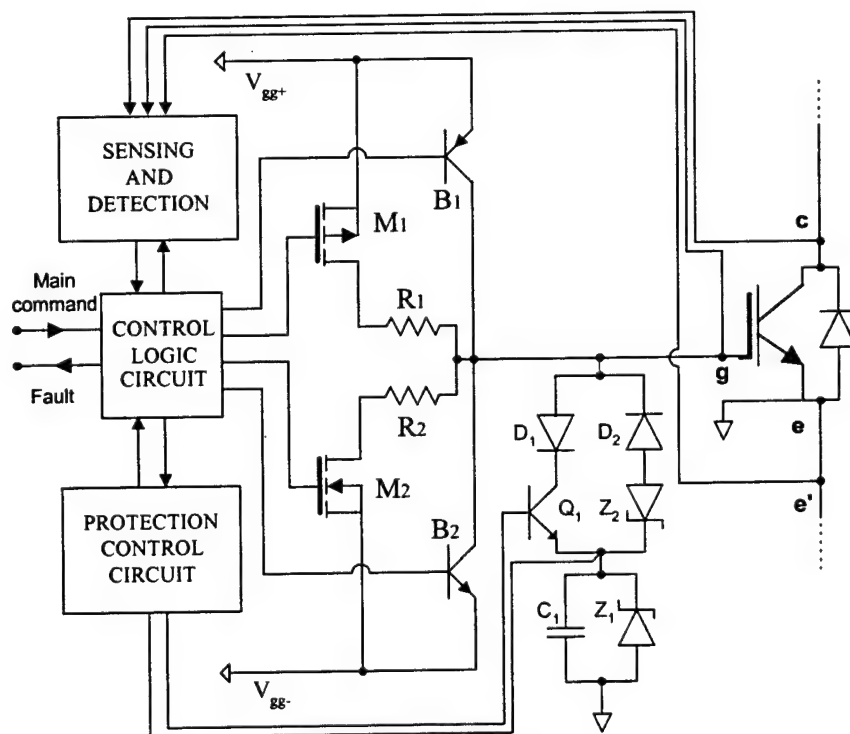


Figure 3-2. Schematic of the three-stage AGD and protection circuit.

Hence, the three-stage AGD continues in stage I rapidly discharging the gate and reaching the off-state gate bias voltage (V_{gg}). De-saturation voltage detection Combined with voltage monitoring, between the Kelvin and power emitter terminals of the IGBT module protects against a short circuit fault. The de-saturation detection is enabled from the end of the stage III of the active turn-on and the monitoring of the v_{ee} is enabled from the start of current rise in the IGBT. The reduced total turn-on duration of the three-stage AGD results in a wider timespan in which faults can be monitored.

3.3 Implementation and Testing

A simplified schematic of the three-stage AGD integrated with the protection circuit is shown in Figure 3-2. The gate amplifier has MOSFETs and BJTs, which are used in parallel to provide the gate current at both turn-on and turn-off switching operation. The use of MOSFETs M_1 and M_2 in the gate drive facilitates obtaining the peak gate current required for fast switching during stages I and III. Resistors R_1 and R_2 are small and are only large enough to just provide damping in the gate circuit. Also, using a MOSFET allows rail-to-rail operation as well as full utilization of the gate power supply voltage. The BJTs B_1 and B_2 allow gate current control during stage II of the switching transient. During short circuit, a combination of capacitor C_1 and zener Z_1 is used to reduce the gate voltage, for fault current limiting. After the fault, the capacitor rapidly discharges the gate and the zener clamps the gate voltage.

A leg of a hard-switched voltage source inverter circuit is used to validate the integrated AGD and protection circuit. The test setup schematic is shown in Figure 3-3. A low-inductance co-axial current transformer is used to measure the device current, which limits the overall parasitic inductance on the DC bus to less than 80nH. A two-pulse method is used to drive the IGBT with an inductor as the load. The time duration for the first pulse is controlled in order to obtain the desired load current, which would be the initial value at turn-on of the second pulse. In case of the fault test a short circuit is applied across the upper device before applying the gate pulse to the device under test (DUT), which is the lower IGBT in the test setup. Both the upper and lower device are mounted on a hot plate. Temperature can be varied from room temperature to the

maximum specified by the data sheets. While a previous test was carried out using Powerex PT IGBT modules (CM600HA-24H 1200V, 600A)[9], the experiments reported here were conducted with Semikron NPT IGBT modules (SKM500G123DS 1200V, 510A).

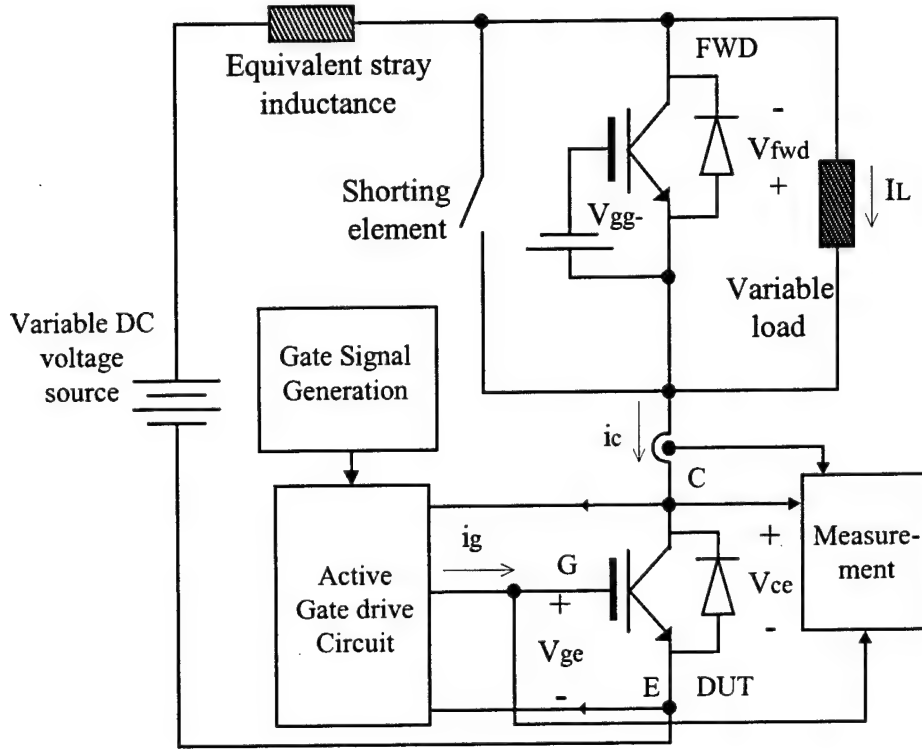


Figure 3-3. The experimental setup used for investigating the gate drive circuit.

3.4 Active Turn-on

The active turn-on sequence is controlled to realize a number of objectives. The turn-on is initiated by switching on M_1 and biasing B_1 in the active region. The turn-on delay and overall switching time is minimized by the peak current provided by M_1 . Once the gate voltage reaches the threshold voltage M_1 is turned off. The gate current is now provided by B_1 , which is biased in the active region to provide a controlled gate current. The turn-on di/dt is controlled to reduce the magnitude of the reverse recovery current. Stage III is initiated by detecting the change in di/dt at the end of the current rise, which corresponds to the snap-off of the freewheeling diode in the hard-switched voltage source power converter. The rate of change of the collector current is detected in the three-stage AGD by sensing the voltage between the Kelvin and power emitter of the IGBT module. After

the snap-off of the freewheeling diode, M_1 is turned on again. The gate Miller plateau duration is reduced by injecting additional current into the gate during turn-on stage-III. The switching loss is lowered by reducing the tail voltage by shortening the Miller Plateau duration. This also reduces the total turn-on switching duration. Figure 3-4 (a) shows collector voltage and current, gate voltage and current and the switching energy during the three-stage turn-on switching transient. If the IGBT is turning on into a fault situation, stage II controls the turn-on di/dt , which limits the peak fault current. In this case, the protection circuit is activated, which limits the fault current level by reducing the gate voltage. Stage III of turn-on is activated only if the DC bus voltage falls below a pre-set threshold voltage. Under fault conditions the current continues to rise without a snap-off of the reverse recovery diode and the collector voltage does not settle to the on-state saturation value. This results in stage III of turn-on being inhibited in the gate drive circuit. This in turn prevents rapid rise in collector current during the turn-on operation under short circuit fault conditions.

3.5 Active Turn-off

When the IGBT is in the on-state, the turn-off command is typically given by the pulse width modulation (PWM) controller in the power converter. The exception is the situation of fault turn-off, when this command can either be given by the system controller in response to the fault signal or internally generated by the gate drive if the fault condition continues beyond the fault endurance duration of the IGBT. A three-stage approach is used for normal turn-off to obtain minimal delay and switching loss while limiting the peak collector voltage. Figure 3-4(b) shows the collector voltage and current and gate voltage and current during a three-stage turn-off switching of the IGBT. The activation of stage II of active turn-off is implemented by monitoring the de-saturation of collector voltage. In case of fault situations, the collector voltage is already de-saturated with the collector voltage close to the DC bus voltage. This eliminates stage I of turn-off and the gate drive proceeds directly to stage II. The reduced gate current during stage II of the active turn-off provides soft shut-down of the IGBT. Hence, both fault turn-off and nominal turn-off follow the same strategy without conflict.

3.6 Temperature Variation

The adaptation of the three-stage AGD with temperature variation of the IGBT and freewheeling diode has been validated in the range from 24°C to 125°C, which is a typical temperature range experienced by these devices in power converters. The current rise in the IGBT starts when the gate voltage goes above the threshold voltage. Hence, the transition point from stage I to stage II (P_{1on}) depends on the operating temperature. The threshold voltage of the MOS gate decreases with increasing temperature [12]. If fixed timing is used to determine the P_{1on} transition, the maximum operating temperature should be used to tune the gate drive for turn-on. The turn-on di/dt depends on the rate of charging of the gate capacitance and the transconductance of the MOS channel of the IGBT. The reduction in mobility with increasing temperature adversely affects the transconductance of the MOS gate.

The stored charge in the diode increases with temperature. This results in larger reverse recovery current and longer current rise duration during turn-on. The decision to transition from stage II to stage III (P_{2on}) is based on sensing the current rise duration. Hence, the three-stage AGD adjusts the duration of stage II, which adapts to the effect of temperature on the diode reverse recovery, as in Figure 3-4(a).

Figure 3-5 (a) and (b) show the trends obtained using the test setup for the IGBT and the freewheeling diode with the three-stage AGD at turn-on. The measurements indicate that temperature has no significant effect on the variation of threshold voltage or transconductance. However, there is a substantial change in the reverse recovery current with variations in temperature, there is larger turn-on loss at higher temperatures.

As the temperature of an IGBT increases the minority carrier lifetime in the drift region has been found to increase [12]. This not only slows down the recombination process but it increases the internal pnp transistor gain of the IGBT.

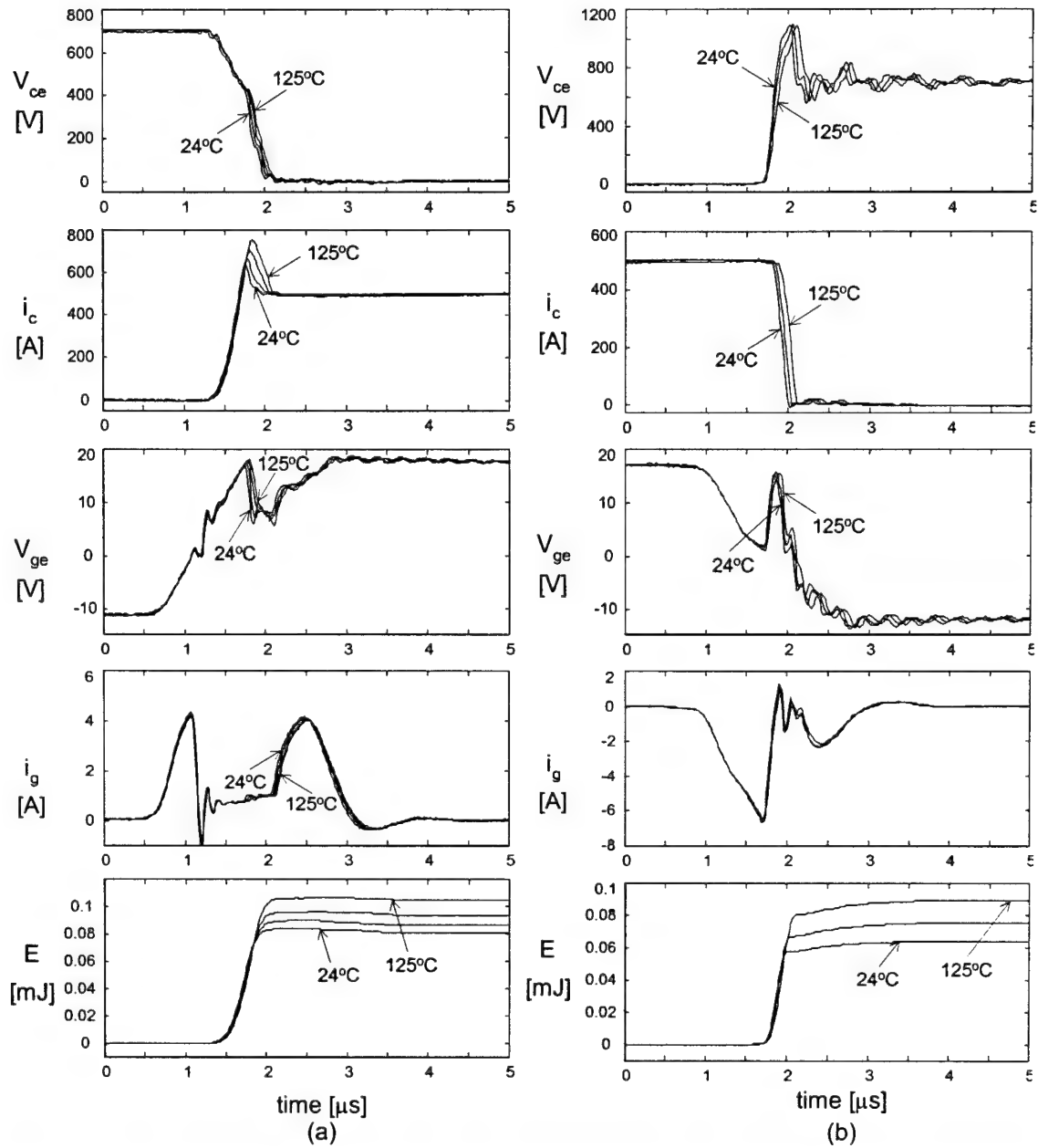


Figure 3-4. Switching waveforms of an IGBT with the three-stage AGD showing collector voltage and current, gate voltage and current, and switching energy as temperature is varied from 24°C to 125°C. (a) Turn-on with $T = 24, 60, 100$ and 125°C. (b) Turn-off with $T = 24, 60$ and 125°C. The operating conditions are $V_{dc} = 750V$ and $I_L = 500A$, $V_{gg+} = 18V$ and $V_{gg-} = -12V$.

The reduction of threshold voltage and transconductance can manifest itself as an increase in the turn-off delay time with an increasing temperature. This can affect the transition from stage I to stage II (P_{loff} control point) in the AGD. The P_{loff} transition in the three-stage AGD is based on the rise in collector voltage at turn-off. This compensates for the variation of turn-off delay time with temperature. The small increase

in T_{doff} with temperature can be seen in Figure 3-4(b) and Figure 3-6(a). At higher temperatures the turn-off dv/dt is reduced for a given current level because of the larger stored charge in the IGBT drift region. The reduction of turn-off dv/dt and di/dt with an increase in temperature leads to higher turn-off switching energy loss as in Figure 3-6(b).

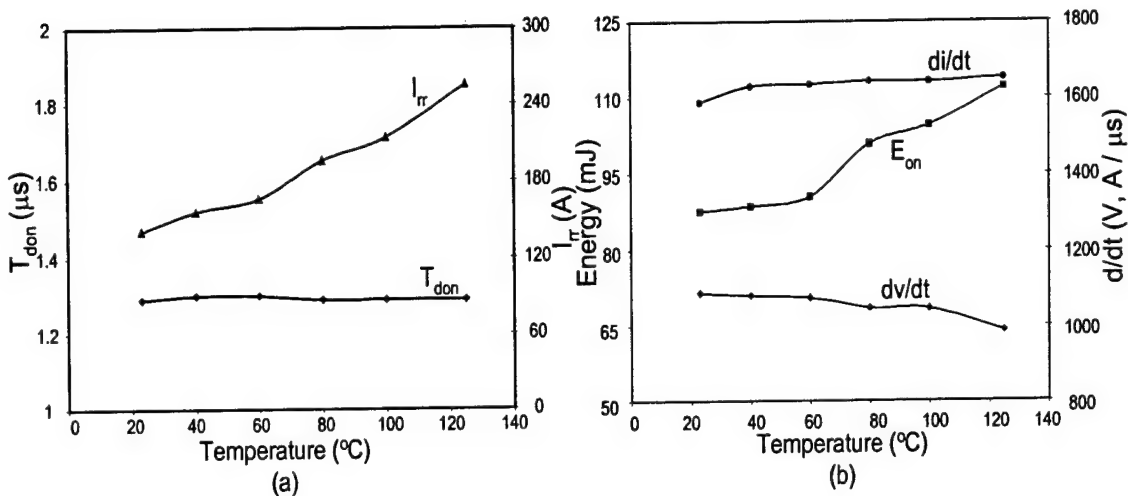


Figure 3-5. Effect of temperature on the IGBT and freewheeling diode at turn-on. (a) The variation of reverse recovery and turn-on delay time. (b) Variation of di/dt , dv/dt and switching energy at turn-on. The measurements are carried out on the Semikron IGBT under operating conditions of $V_{\text{dc}} = 750\text{V}$ and $I_L = 500\text{A}$, $V_{\text{gg}^+} = 18\text{V}$ and $V_{\text{gg}^-} = -12\text{V}$.

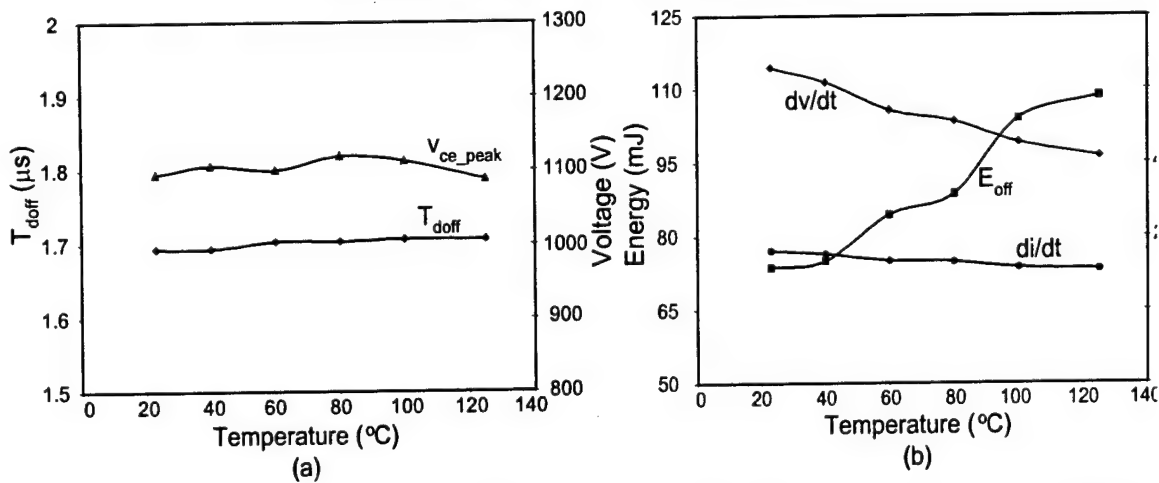


Figure 3-6. Effect of temperature on the IGBT and freewheeling diode at turn-off. (a) The variation of peak voltage and delay time at turn-off. (b) Variation of dv/dt , di/dt , and switching energy at turn-off. The measurements are made using the Semikron IGBT under operating conditions of $V_{\text{dc}} = 750\text{V}$ and $I_L = 500\text{A}$, $V_{\text{gg}^+} = 18\text{V}$ and $V_{\text{gg}^-} = -12\text{V}$.

The result of the re-turn-on of the gate during active turn-off is larger stored charge, which results in a larger current tail at higher temperature. Hence, the turn-off switching energy that increases with temperature increases more rapidly in an AGD than in a conventional gate drive.

3.7 Fault Handling

Detection of the fault is performed using a combination of de-saturation detection and estimation of the device current level using the voltage between the Kelvin and power emitter terminals of the IGBT. The transition from the controlled current rise in the IGBT to the turn-on steady state is performed only if no fault signal is detected. If there is a short circuit condition at turn-on, the protection circuit reduces the gate voltage and limits the fault current level, thus reducing the power dissipation during a fault. This allows us use of a higher on-state gate voltage for the device, which results in a lower conduction voltage drop. The main control circuit of the power converter is given the fault signal, and the gate drive turns off within the short circuit endurance time of the IGBT. The short circuit protection has to be coordinated with over-temperature protection to prevent failure due to repeated operation under fault conditions.

The power converter's ability to ride through and survive an over-current or short circuit fault can be enhanced using a gate drive that can limit the fault currents. The use of a higher gate voltage can be dangerous under short circuit and over-current conditions because the resulting higher fault current can lead to large power dissipation that can destroy the IGBT. It has been shown that a combination of a capacitor and zener based FCLC can be effective in limiting both the peak and clamped fault current levels [7]. Lowering the gate voltage under fault conditions instead of using direct turn-off prevents the inductive turn-off failure that can occur under peak fault current level [13], [14]. The fault current has to be turned off softly to prevent large IGBT collector over-voltage.

Figure 3-7 (a) illustrates short-circuit fault occurrence with a conventional gate drive without the FCLC and Figure 3-7 (b) shows the three-stage AGD with the FCLC. The gate drive transits from stage II of turn-on to a fault state to prevent large currents under fault conditions. A soft turn-off is required in case of over-current or short-circuit shutdown to prevent large over-voltage from damaging the IGBT. This is achieved by preventing the activation of turn-off stage I and moving directly to stage II of the three-stage active turn-off. The fault turn-off in the conventional gate drive uses a large gate resistance (33Ω), but the turn-off over-voltage is much higher compared to the three-stage AGD (Figure 3-7).

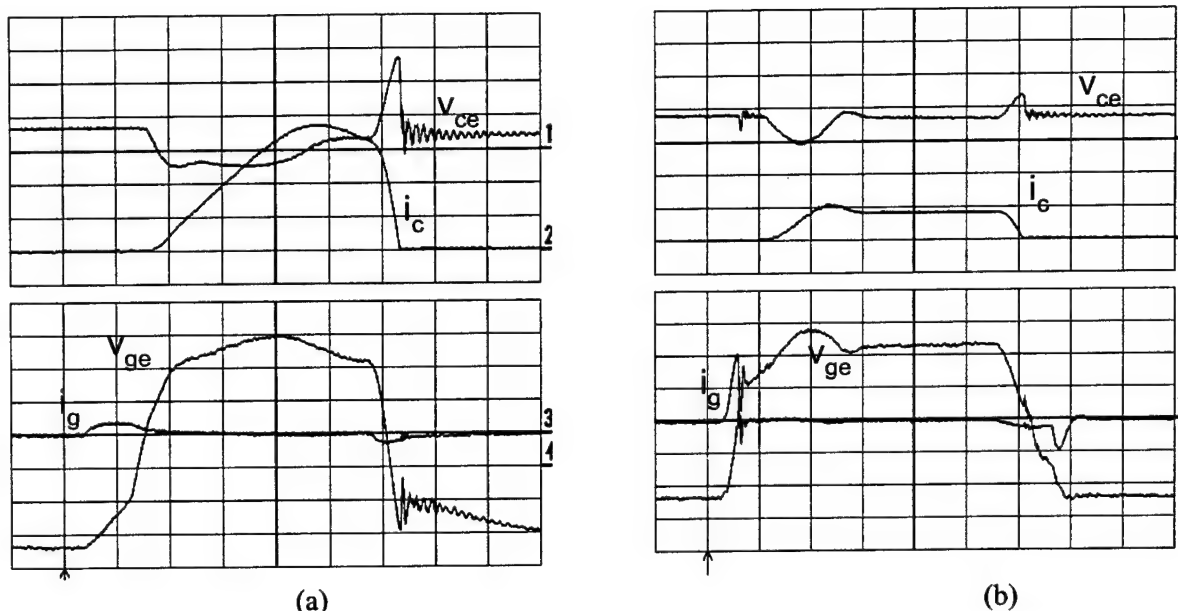


Figure 3-7. Short circuit protection test carried out with the Semikron IGBT module (a) CGD without fault current limiting protection and $R_g = 33\Omega$ (b) AGD with fault current limiting protection. Ch1. V_{ce} : 200V/div, Ch2. i_c : 1000A/div, Ch3. i_g : 2A/div, Ch4. V_{ge} : 5V/div, time: 2ms/div. $V_{dc} = 750V$, $V_{gg+} = 18V$ and $V_{gg-} = -12V$.

3.8 Conclusions

This chapter has discussed issues in the design of a three-stage AGD its different modes of operation, including validating its operation under a wide temperature range of the IGBT and freewheeling diode. The gate drive adapts itself to a wide range of operating conditions. The operation of the gate drive has been tested with IGBT modules from several manufacturers. The three-stage AGD has been integrated with the fast fault current limiting technique to protect the IGBT under fault conditions. Such characteristics are especially important for the high voltage IGBTs that are available today and for standardization of high power IGBT switches in the form of a power electronic building block.

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Chapter 4 Control Strategies for a Hybrid Seven-level Inverter

This chapter is devoted to the investigation of control techniques applicable to a seven-level 4.16 kV hybrid inverter. A detailed analysis of a hybrid modulation technique, which incorporates stepped synthesis in conjunction with variable pulse width of the consecutive steps, is included. In addition, variations of multicarrier pulse width modulation (PWM) techniques related to the disposition and phase shifting and their comparative evaluation are presented in this report. The performance attributes of conventional techniques (such as staircase modulation and programmed PWM) are assessed, and optimization of switching angles to minimize the harmonic distortion at different modulation depths is discussed. Operating principles, spectral structure and other practical issues are studied. Computer simulations accompanied by experimental results are also presented.

4.1 Introduction

Multilevel power conversion has received increasing attention in the past few years for high-power applications [1], [2]. Numerous topologies have been introduced and studied extensively for utility and drive applications. Due to their ability to synthesize waveforms with better harmonic spectrum and attain higher voltages with a limited maximum device rating, these converters are suitable in high voltage and high-power applications.

Recent trends in power semiconductor technology indicate a trade-off in the selection of power devices in terms of switching frequency and voltage sustaining capability [3]. Normally, the voltage blocking capability of faster devices such as IGBT and the switching speed of high voltage devices like the Integrated Gate Commutated Thyristor (IGCT) [4] is found to be limited. With a modular H-bridge topology [5], it is possible to realize multilevel inverters that use a hybrid approach involving synergistically operating IGCTs and IGBTs. Hybrid multilevel inverter topologies have been studied for high-power applications [6]–[10]. A previously presented topology combines a gate turn-off (GTO) thyristor-based inverter and an IGBT inverter, similar to that shown in Figure 4-1, [9]. It may be easily verified that with a combination of 2.2 kV and 1.1 kV DC bus

voltages in this topology, it is possible to synthesize stepped waveforms with seven voltage levels viz. -3.3 kV, -2.2 kV, -1.1 kV, 0 , 1.1 kV, 2.2 kV, 3.3 kV at the phase leg output.

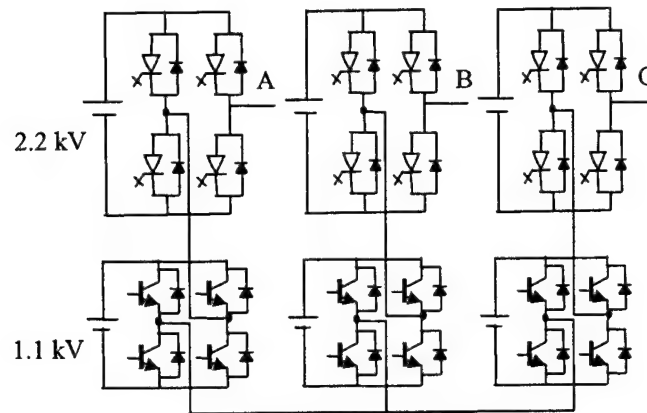


Figure 4-1. Simplified schematic of the hybrid seven-level inverter.

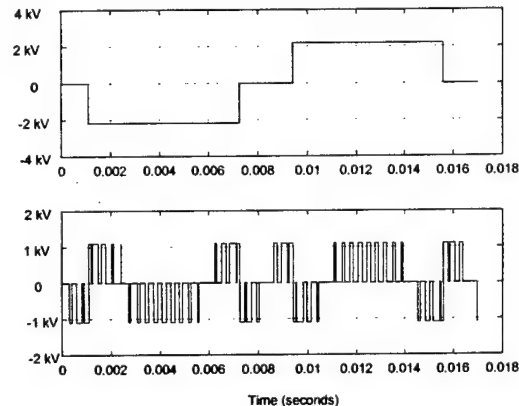
This paper is devoted to an assessment of various modulation strategies applicable to this inverter. A comparative evaluation of these techniques in terms of attributes such as average switching frequency, dominant harmonics and total harmonic distortion (THD) in the output voltage are reported. The following two sections present the development of high switching frequency techniques, for example, hybrid modulation and the conventional sub-harmonic PWM. This is followed by an evaluation of low switching frequency techniques, such as staircase modulation and programmed PWM. The paper concludes with a discussion of advantages and disadvantages of these control strategies.

4.2 Hybrid Modulation Technique

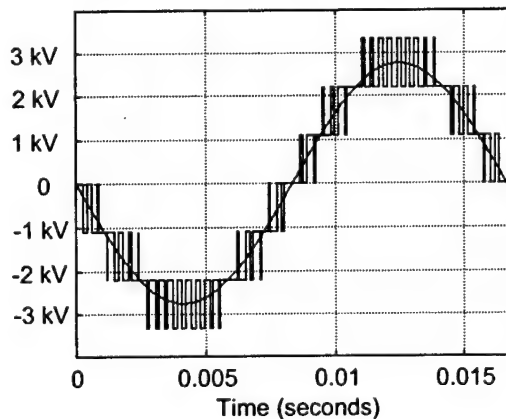
Table I. Hybrid modulation scheme

Desired Output	IGCT Inverter	IGBT Inverter (a \leftrightarrow b : Switching between a and b)
-3.3 to -2.2 kV	-2.2 kV	$0 \leftrightarrow -1.1$ kV
-2.2 to -1.1 kV	-2.2 kV	$0 \leftrightarrow 1.1$ kV
-1.1 to 0.0 kV	0 kV	$0 \leftrightarrow -1.1$ kV
0.0 to 1.1 kV	0 kV	$0 \leftrightarrow 1.1$ kV
1.1 to 2.2 kV	2.2 kV	$0 \leftrightarrow -1.1$ kV
1.1 to 3.3 kV	2.2 kV	$0 \leftrightarrow 1.1$ kV

The motivation behind investigating the hybrid topology is the pursuit of a synergistic approach, which combines the fast switching ability of IGBTs and large voltage blocking capability of IGCTs. As shown in Figure 4-1, the higher voltage levels (± 2.2 kV) are synthesized using IGCT inverters while the lower voltage levels (± 1.1 kV) are synthesized using IGBT inverters. But it is well known that the switching capability of thyristor-based devices is limited at higher frequencies [4]. Hence a hybrid modulation strategy, which incorporates stepped synthesis in conjunction with variable pulse width of consecutive steps, has been presented [9]. Under this modulation strategy, the IGCT inverter is modulated to switch only at fundamental frequency of the inverter output while the IGBT inverter is used to switch at a higher frequency (f_c). The modulation process and the state of the inverters for various levels of command signals is summarized in Table I.

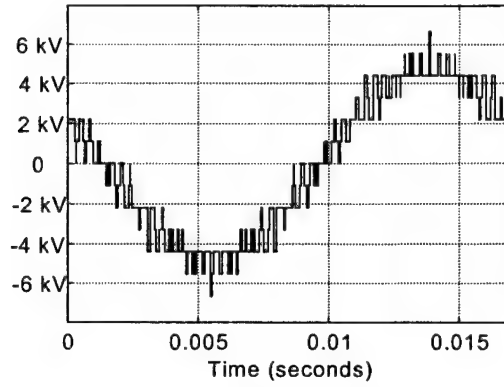


a) IGCT and IGBT inverter voltages.

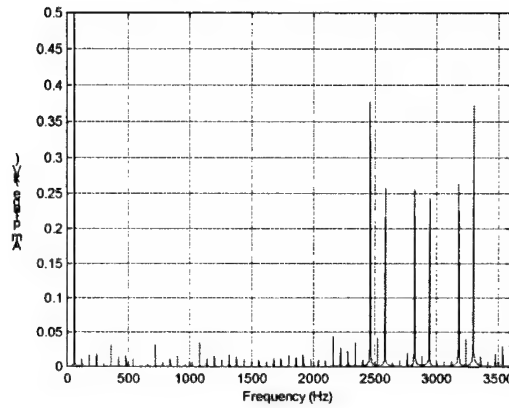


b) Hybrid inverter phase leg voltage.

Figure 4-2. Representative leg waveforms for hybrid modulation, $M = 0.83$ and $f_c = 1440$ Hz.



a) Line-line voltage.



b) Harmonic spectrum of the line-line voltage.

Figure 4-3. Representative line waveforms for hybrid modulation, $M = 0.83$ and $f_c = 1440$ Hz.

With this hybrid modulation strategy, the effective spectral response of the output depends on the IGBT switching, while the overall voltage generation is decided by the voltage ratings of the IGCTs. This is illustrated in Figure 4-2. Figure 4-3 shows line-line voltage waveform and harmonic spectrum for the same operating point. As expected, the harmonic power is clustered at the side bands at twice the switching frequency, which is 1440 Hz.

For spectral analysis, reference command to the hybrid inverter can be represented as

$$V_{\text{ref}} = M \cos \omega t \quad (1)$$

where M is the modulation depth, which varies between $0 \leq M \leq 1$, and ω is angular frequency of the reference signal. So the IGCT inverter output and the IGBT inverter leg command are given by

$$V_{IGCT} = \sum \frac{8}{3n\pi} \sin \left\{ n \cos^{-1} \frac{1}{3M} \right\} \cos n\omega t \quad (\text{for odd } n) \quad (2)$$

$$V_{IGBT (\text{command})} = M \cos \omega t - \sum \frac{8}{3n\pi} \sin \left\{ n \cos^{-1} \frac{1}{3M} \right\} \cos n\omega t \quad (\text{for odd } n) \quad (3)$$

Now, the spectrum of a naturally sampled sine-triangle PWM single-phase voltage source inverter (VSI) with a leg command $A \cos \omega_0 t$ and carrier frequency ω_c is given in [11] as follows

$$V_{VSI} = A \cos \omega_0 t + \frac{4}{\pi} \sum \sum \frac{1}{2m} J_{2n-1} A m \pi \cos \{ 2m \omega_c t + (2n-1) \omega_0 t \} \quad (4)$$

(Summations from $m = 1$ to ∞ and $n = -\infty$ to $+\infty$)

One can substitute Equation (3) in (4) and obtain a complete spectrum for the PWM IGBT inverter. When added to the spectrum of the IGCT inverter [Equation (2)], this gives a complete spectrum of the hybrid inverter. It may be noted from Equation (4) that there exists a term $A \cos \omega_0 t$ in the spectrum of the VSI output when modulated with a reference $A \cos \omega_0 t$. Hence the low frequency harmonics generated by the IGCT inverter will be cancelled by the corresponding terms in the spectral output of the IGBT inverter, and there will only be side bands at multiples of carrier frequency. This can be verified from the spectrum of the output voltage in Figure 4-3(b).

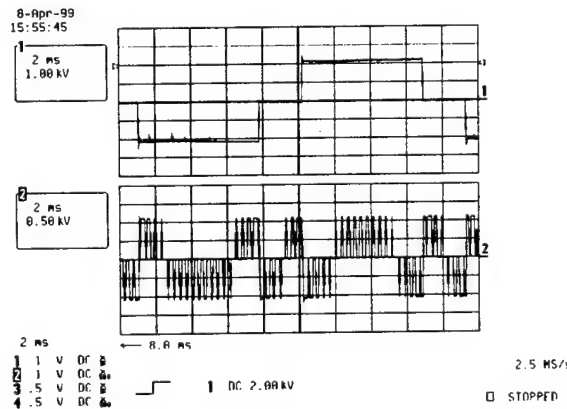


Figure 4-4. Experimental IGCT and IGBT inverter waveforms, $M = 0.83$ and $f_c = 1440$ Hz.

Trace 1. IGCT inverter voltage 1000V/div. Trace 2. IGBT inverter voltage 500V/div.

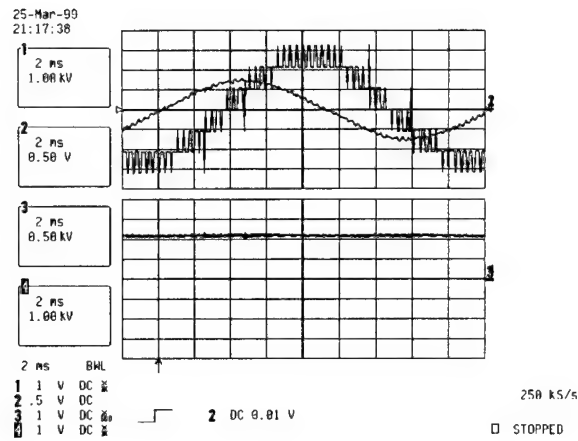


Figure 4-5. Experimental load and DC bus voltage waveforms, $M = 0.83$ and $f_c = 1440$ Hz.

Trace 1. Output voltage 1000V/div. Trace 2. Output current 5A/div.
Trace 3. IGBT DC bus 500V/div. Trace 4. IGCT DC bus 1000V/div.

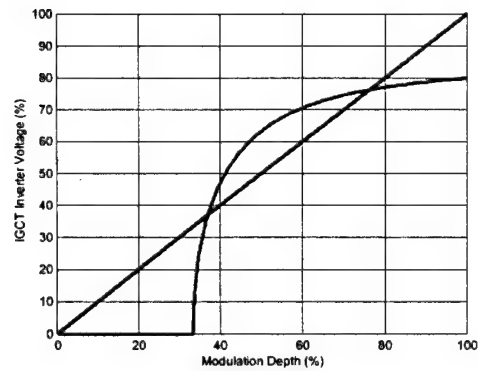


Figure 4-6. IGCT inverter fundamental voltage.

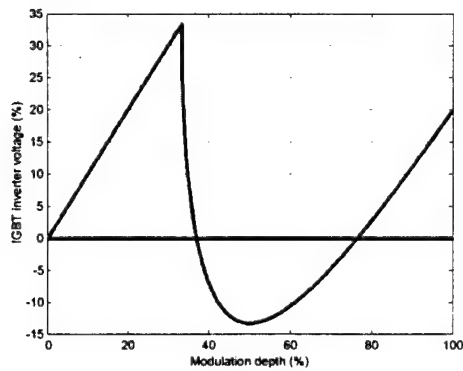


Figure 4-7. IGBT inverter fundamental voltage.

Behavior of the individual inverters at fundamental frequency is particularly interesting. The IGCT inverter output under hybrid modulation is plotted against the modulation depth in Figure 4-6. It is overlaid on a unity slope line, which specifies the commanded fundamental voltage. It may be observed that the IGCT inverter synthesizes more voltage than necessary between the modulation depths around 37% and 78%. Hence it is necessary for the IGBT inverter to cancel this excessive voltage, as illustrated in Figure 4-7. As shown by the fundamental voltage synthesized by the IGBT inverter, this inverter synthesizes negative voltage in this region of modulation depths. In terms of real power flow, which is represented by the current component that is in phase with the fundamental voltage, it appears that the IGCT inverter feeds the power into the IGBT inverter in this zone.

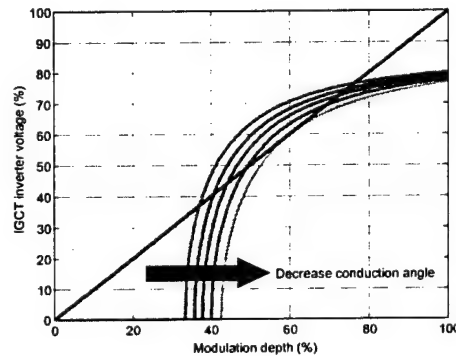


Figure 4-8. Conduction angle control of the IGCT inverter.

A simple solution for this problem is to control the conduction angle of the IGCT inverter such that the fundamental voltage generated by this inverter is always less than the total commanded voltage. In this mode, the IGBT inverter always adds the voltage and never has to regenerate the power flow. This control scheme is illustrated in Figure 4-8. In the original hybrid modulation strategy, the IGCT inverter starts contributing as soon as the command reaches 0.33 p.u. As seen in Figure 4-8, this contribution switching time is delayed in terms of modulation depth so as to narrow down the pulse width, thereby decreasing the synthesized fundamental voltage. Although this solution does solve the problem of power interaction between the two inverters, it suffers from a higher harmonic distortion than the original hybrid modulation scheme. Simulation and experimental work to verify the feasibility of this approach is under way and will be reported in the near

future [12]. A more sophisticated version of the solution to this problem, involving a regenerative rectifier, is treated in a separate publication [13].

4.3 Sub-harmonic Pulse Width Modulation (SPWM) Technique

Conventional SPWM strategies for multilevel inverters employ extensions of carrier-based techniques used for two-level inverters. It has been reported that the spectral performance of a five-level waveform can be significantly improved by employing alternative dispositions and phase shifts in the carrier signals [14], [15]. This paper extends this concept to a seven-level case where the available options for polarity and phase variation increase nearly two-fold. Basically, the SPWM techniques can be broadly categorized into two groups: carrier polarity variation and carrier phase variation.

Carrier Polarity Variation (Pol. Var.): This method involves a comparative evaluation of possible dispositions of triangular carrier waveforms, based on their relative polarities. For an m -level inverter, this technique requires $m-1$ carrier signals, which are compared to a reference sine wave. Thus, for a seven-level inverter, the number of carrier signals is six and there exist five possible carrier signal configurations. The carriers are named after their DC position, +3V, +2V, +V, -V, -2V and -3V. Their phase position is positive for a carrier in phase and negative for a carrier 180° out of phase. The different configurations are shown in Table II.

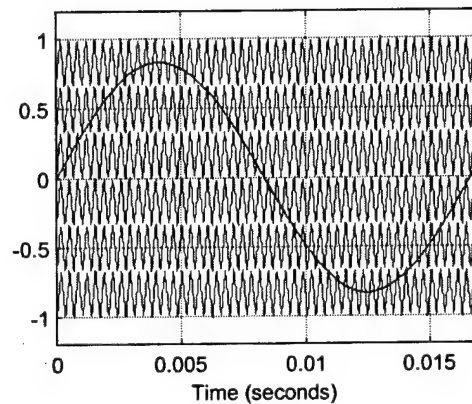
Table II: Carrier polarity configurations for a seven-level modulator.

	Carrier Polarity					
	+3V	+2V	+V	-V	-2V	-3V
A	+	+	+	+	+	+
B	+	-	+	-	+	-
C	+	+	+	-	-	-
D	+	-	-	+	+	-
E	+	+	-	+	-	-

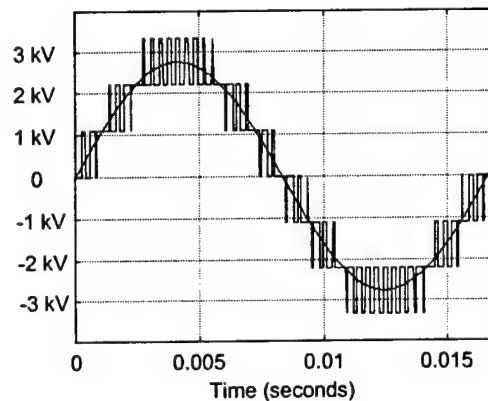
This table presents five possible dispositions of triangular carrier waveforms, based on their relative polarities. The type A carriers all have the same polarity, while the type B carriers have alternative polarity. In type C, all the positive carriers have the same relative

polarity but are in opposition to those below zero. Types D and E are additional variations of the carrier signal configurations.

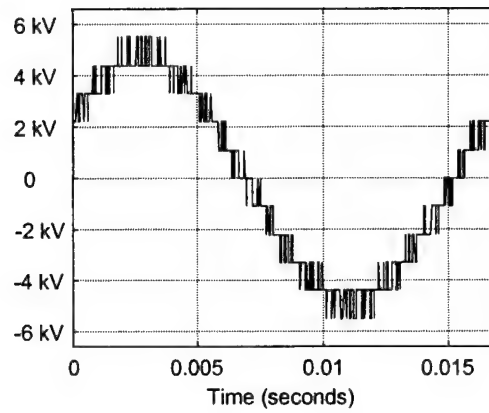
All the different polarity variations are simulated in MATLAB Simulink. Simulation studies indicate that the spectral structure of the output with each pattern of carrier disposition is different and a small difference in the respective THD values has been observed. A representative SPWM waveform is shown in Figure 4-9. The spectral power is spread out around the carrier frequency and the harmonics are clustered at the side bands.



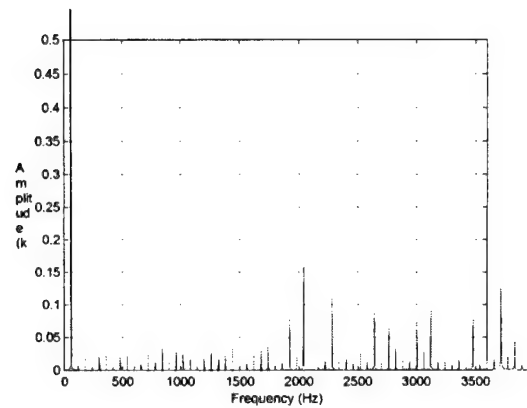
a) Reference and carrier signals.



b) Phase leg voltage.

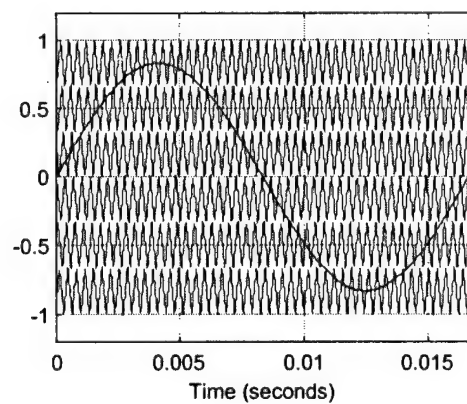


c) Line-line voltage.

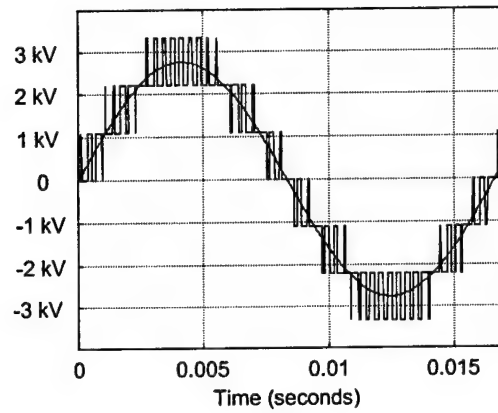


d) Harmonic spectrum of the line-line voltage

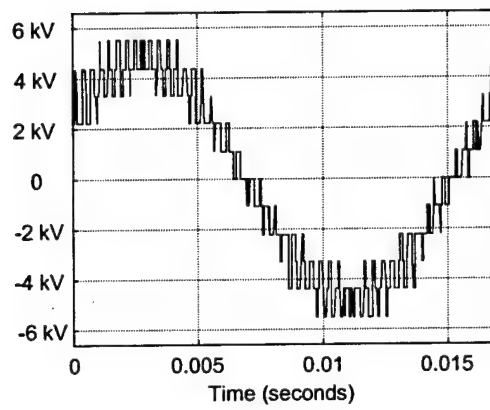
Figure 4-9. Representative waveforms for SPWM with Type A carrier polarity variation, $M = 0.83$ and $f_c = 1440$ Hz.



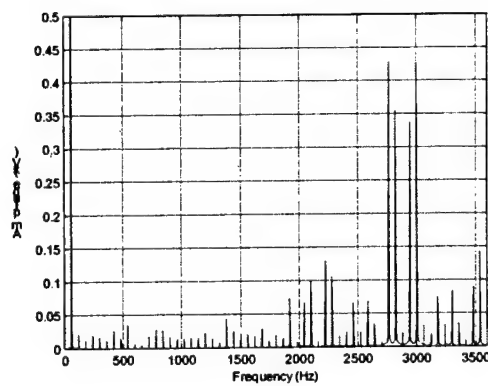
a) Reference and carrier signals.



b) Phase leg voltage.



c) Line-line voltage.



d) Harmonic spectrum of the line-line voltage

Figure 4-10. Representative waveforms for SPWM with carrier phase variation, $M = 0.83$ and $f_c = 1440$ Hz.

Carrier Phase Variation (Phase Var.): This technique uses a number of carriers that are phase shifted with each other. For a seven-level inverter six carrier signals are phase shifted by 60° (Figure 4-10). The spectral structure is different from the carrier polarity variation presented in Figure 4-9. Also, the output voltage and current THD compare unfavorably with other SPWM techniques.

4.4 Staircase Modulation Technique

A simple seven-level staircase waveform at the phase leg output with the candidate hybrid topology can be synthesized (Figure 4-11). As may be observed from Figure 1, the inverters can synthesize 0, ± 1.1 kV and ± 2.2 kV independently. In addition, levels ± 3.3 kV can be obtained by combining ± 1.1 kV and ± 2.2 kV. Although this strategy is not particularly attractive in terms of spectral quality, it is desirable to operate the inverter in such overmodulation regions for improved DC bus and device utilization. Also, this strategy needs only low switching frequency capability from the devices. However, it is possible to optimize the switching angles of the individual inverters (α_i) for a given modulation index M , so as to minimize a set of dominant harmonics in the output [16].

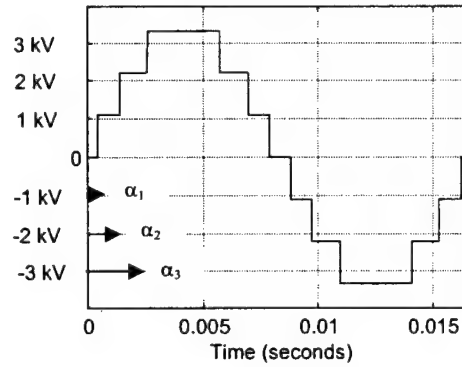


Figure 4-11. Staircase modulation and definition of switching angles.

To obtain an optimization cost function, the Fourier coefficients of the output voltage can be derived as follows

$$H(n) = V_{dc2} \frac{4}{\pi} \frac{1}{n} [\cos(n\alpha_1) + \cos(n\alpha_2) + \cos(n\alpha_3)] \quad (5)$$

where $V_{dc2} = 1.1$ kV and $n = 1, 3, 5, 7, \dots$

If all the switching angles are set to zero, the output falls back to a conventional two-level waveform, and the fundamental voltage in this case is given by

$$H_{\max}(1) = 3 V_{dc2} \frac{4}{\pi} \quad (6)$$

Since there are three degrees of freedom (three α_i 's), three independent parameters can be simultaneously controlled. The maximum attainable fundamental voltage with elimination of the first three harmonics (5^{th} , 7^{th} and 11^{th}), is 92% of $H_{\max}(1)$. For lower values of fundamental voltage, solving Equations (7)-(9) gives switching angles to eliminate the 5^{th} and 7^{th} harmonic components. It may be noted that 5^{th} and 7^{th} are the most dominant harmonics, since the even harmonics are cancelled because of the elimination of half-wave symmetry and triplen harmonics in a three-phase three-wire system.

$$H(1) = 3 V_{dc2} M, \quad (7)$$

$$H(5) = 0 \text{ and} \quad (8)$$

$$H(7) = 0, \quad (9)$$

$$\text{where } 0 \leq M \leq \frac{4}{\pi}$$

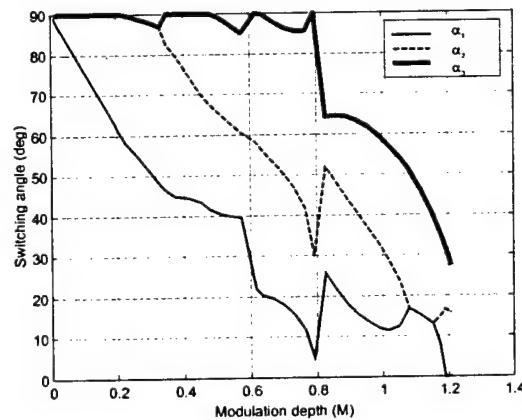


Figure 4-12. Switching angles for staircase modulation as a function of modulation depth.

To solve equations (7)-(9), a previously described technique can be used [17]. Suppose a vector of angles $\alpha = [\alpha_1, \alpha_2, \dots, \alpha_n]^T$ satisfies a set of equations $H_i(\alpha) = 0$ to be solved. Then one can formulate an equivalent minimization problem as follows:

$$F(\alpha) = \sum_{i=1} [H_i(\alpha)]^2 \quad (10)$$

$F(\alpha)$ is always non-negative, and therefore, if values of α exist for which $F(\alpha) = 0$, these have to be the minimum points for $F(\alpha)$. When $F(\alpha)$ is zero, each $H_i(\alpha)$ must be zero, thus the solution of the set of the equations is to search for the minima of Equation (10). This is done by using the MATLAB optimization toolbox. The results of the simulations are given in the graphs presented in Figure 4-12.

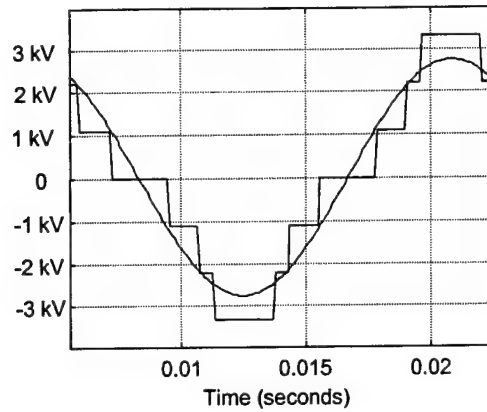
As the modulation depth approaches $4/\pi$, the switching angles approach zero, which results in a conventional six-step inverter waveform. As the modulation depth decreases, the switching angles approach 90° one by one, which means the phase leg voltage converts from seven-level to five-level and eventually to three-level mode.

A representative staircase modulated waveform is shown in Figure 13. The 5th (300 Hz) and the 7th (420 Hz) harmonics are eliminated from the harmonic spectrum of line-line voltage.

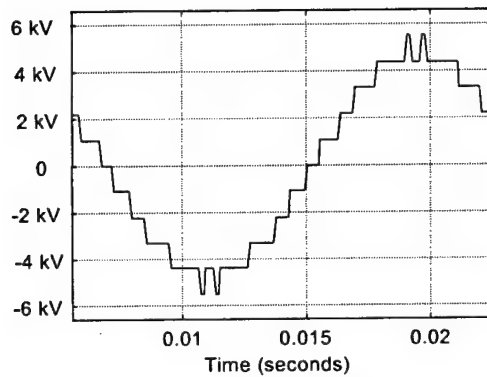
The PPWM technique was originally proposed for the conventional two-level inverters [18] and has been extended to multilevel inverters [19], [20]. The basic concept of PPWM is to introduce notches on the staircase and eliminate some more harmonics, which are a function of the position and width of the notch. A simplest option is to introduce one notch at the top level as shown in Figure 4-14. To obtain an optimization cost function, the Fourier coefficients of the output voltage can be derived as follows:

$$H(n) = V_{dc2} \frac{4}{\pi} \frac{1}{n} [\cos(n\alpha_1) + \cos(n\alpha_2) + \cos(n\alpha_3) + \cos(n\alpha_4) - \cos(n\alpha_5)], \quad (11)$$

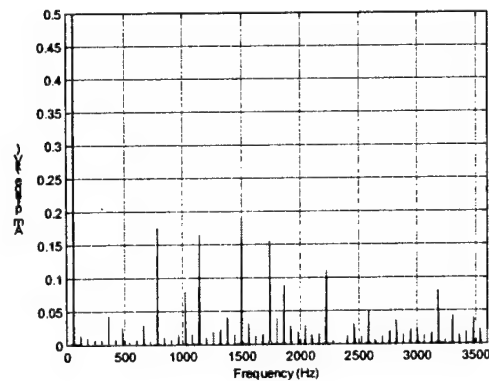
where $V_{dc2} = 1.1$ kV and $n = 1, 3, 5, 7, \dots$



a) Phase leg voltage.



b) Line-line voltage.



c) Harmonic spectrum of the line-line voltage.

Figure 4-13. Representative waveforms for staircase modulation with optimized switching angles to eliminate 5th and 7th harmonic components, $M = 0.83$.

Programmed Pulse Width Modulation (PPWM) Technique

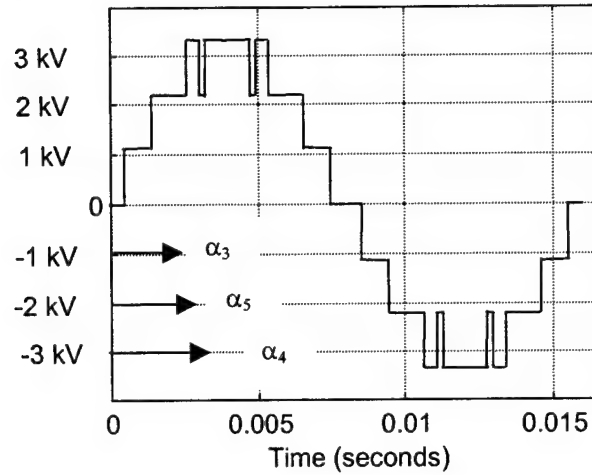


Figure 4-14. PPWM and definition of switching angles.

Since there are five degrees of freedom (five α_i 's), five independent parameters can be simultaneously controlled. It is required to solve Equations (12)-(16) for switching angles to eliminate the 5th, 7th, 11th and 13th harmonic components to synthesize the fundamental voltage with a given modulation depth. Although it is possible to introduce more notches in order to cancel more harmonics, the process is computation-intensive and the law of diminishing returns sets in quickly with the increasing number of notches. Moreover, it has been observed that elimination of 5th, 7th, 11th and 13th harmonics is sufficient to obtain a satisfactory level of THD in the output current at high-power levels.

$$H(1) = 3 V_{dc2} M, \quad (12)$$

$$H(5) = 0, \quad (13)$$

$$H(7) = 0, \quad (14)$$

$$H(11) = 0, \quad (15)$$

$$H(13) = 0, \quad (16)$$

$$\text{where } 0 \leq M \leq \frac{4}{\pi}$$

The equations are solved by the previously described procedure, and the results are presented in Figure 4-15. The typical time and frequency domain waveforms are shown

in Figure 4-16. The 5th (300 Hz), 7th (420 Hz), 11th (660 Hz) and 13th (780 Hz) harmonics are eliminated from the harmonic spectrum of line-line voltage.

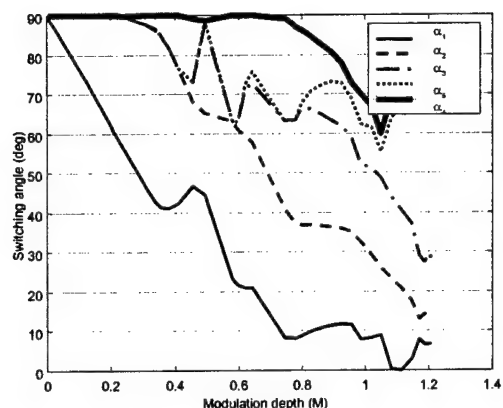
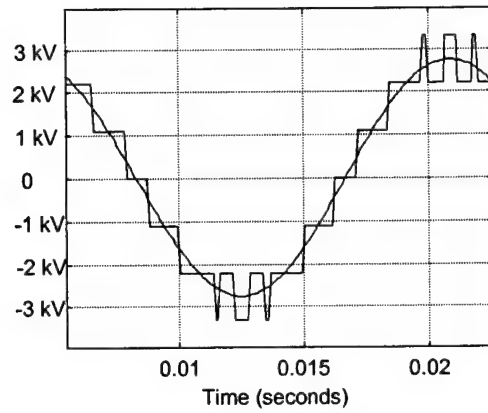
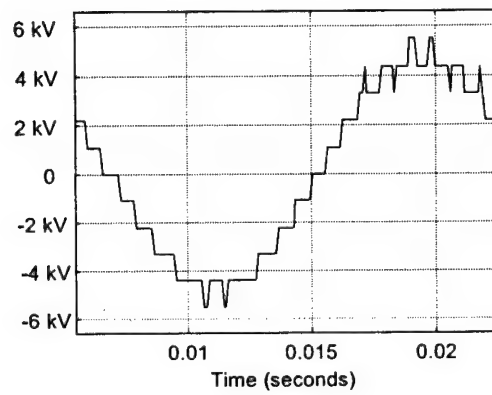


Figure 4-15. Switching angles for PPWM as a function of modulation depth.

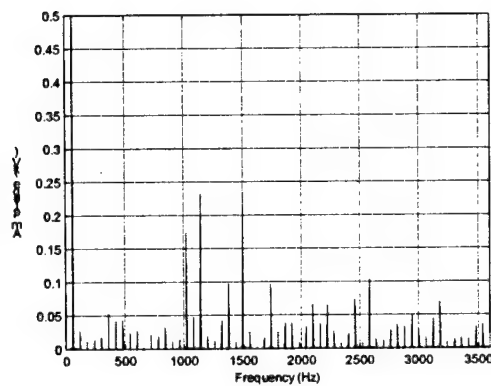
Figure 4-12 and Figure 4-15 show that seven-level staircase modulation is suitable in modulation depths from 0.8 to 1.2, whereas PPWM is suitable in region $0.8 \leq M \leq 1.0$. Simulation results presented so far are done with constant frequency, which is a typical case in utility applications. Also, unlike variable frequency drives, such applications normally operate only in a limited range at the higher modulation depths. Hence the simulation results presented so far validate that the hybrid multilevel inverter can be employed for utility applications such as reactive power compensation with PPWM in linear regions and with staircase modulation in overmodulation regions. On the contrary, for drive applications such as constant V/Hz drives, the output fundamental frequency decreases with the output voltage. Hence it is possible to introduce more notches at the lower frequency, thereby eliminating harmonics, while maintaining a constant overall switching frequency. By this reasoning, one can optimize the PPWM patterns further at lower modulation depths in such cases. But this optimization is application specific and hence not considered in detail here.



a) Phase leg voltage.



b) Line-line voltage.



c) Harmonic spectrum of the line-line voltage.

Figure 4-16. Representative waveforms for PPWM with optimized switching angles to eliminate 5th, 7th, 11th and 13th harmonic components; $M = 0.83$.

4.5 Conclusions

This paper has presented a comparative evaluation of various control strategies applicable to the hybrid seven-level inverter. Superior performance attributes, in terms of voltage THD with low frequency techniques such as staircase and PPWM, can be obtained. However, since these strategies optimize the waveforms for a particular set of harmonics, the dominant harmonics are still at low frequencies. On the contrary, the dominant harmonics present in the high-frequency techniques are at the side bands of multiples of the switching frequency, but the voltage THD in these cases is relatively poor. A comparison of these techniques is tabulated in Table III.

Compared with other control strategies, application-specific PPWM techniques offer excellent THD figures. With sufficient numbers of harmonic elimination notches, the dominant harmonic component can be pushed in high-frequency region. Thus, it is possible to obtain a satisfactory spectral performance with relatively low switching frequency.

Table III. Comparison of control strategies.

Modulation Technique	$V_{\text{line-line}}$ THD (%)	Dominant Harmonic (Hz)
Hybrid	12.9998	2460 (41 st)
Pol. Var. SPWM	8.5260	2040 (34 th)
Phase Var. SPWM	14.6078	2760 (46 th)
Staircase	6.3573	780 (13 th)
PPWM	7.1880	1020 (17 th)

4.6 References

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Chapter 5 Simulation of the Hybrid Multilevel Inverter System

5.1 Introduction

The sizing of power components for a real hybrid seven-level inverter rated for a 4.16 kV, 100 HP drive was described in the previous chapter. The preliminary simulation results presented therein confirmed the feasibility of the hybrid approach studied in this work. This chapter describes the models and presents the results of circuit simulations of the hybrid inverter in Saber.

The following section first describes the model of the power circuit built in Saber. This includes the power input stage, device bridges and load. It is followed by a description of a model of the hybrid modulator. Section 3.3 presents simulation results of the hybrid multilevel inverter operating at various modulation depths. Finally, detailed simulation results of the inverter operating at modulation depth $M = 0.83$ are given in Section 3.4.

5.2 Circuit Modeling

Figure 5-1 illustrates the model of a single leg of the hybrid seven-level inverter. The model can be grouped into the following: power input stage, intermediate DC link and power output stage; device bridges; and modulator. The supply voltage is set at 480V rms which feeds the two isolation / step-up transformers.

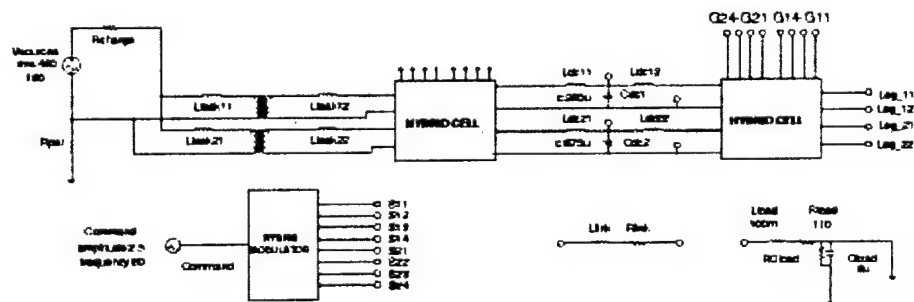


Figure 5-1. Circuit schematic of the model for one leg of the hybrid seven-level inverter.

As there is a possibility of oscillations between the DC link capacitor and leakage inductance of these transformers, a charge-up resistance is added to damp the resonant currents. The transformer model parameters used in the simulations are given in Table 8.

The DC links are composed of bus capacitors and parasitic inductors, which link the two device bridges. A 24 kVA passive load is represented by a 110 W resistance, 100 mH inductance and 8 mF capacitance.

Table 8. Simulation parameters used to model the transformers

Parameter	LV Transformer	HV Transformer
Primary Turns	135	88
Primary Resistance	100m Ω	100m Ω
Secondary Turns	256	334
Secondary Resistance	100m Ω	100m Ω
Magnetic Path Length	0.61m	0.93m
Cross Sectional Area	0.0103m ²	0.0154m ²
Coupling Coefficient	1	1

The device bridges are shown in Figure 5-2. This figure shows two single-phase H-bridge inverters connected to one high voltage and one low voltage DC link. Switches S_{11} - S_{14} correspond to IGCTs, while switches S_{21} - S_{24} are the corresponding IGBTs. The device models use default parameters specified by Saber.

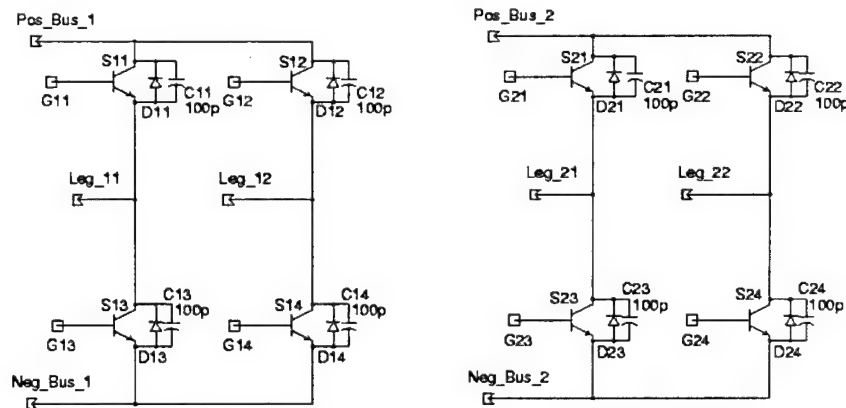


Figure 5-2. Circuit schematic of the model for the device bridges in hybrid inverter.

Figure 5-3 illustrates the modulator modeled in Saber. The modulation scheme follows the strategy described in Chapter 2. A crude version of the implementation can be devised as follows: When an inverter is required to produce positive / zero outputs, switches S_{x1} - S_{x4} / S_{x2} are closed. When an inverter is required to synthesize negative / zero outputs, switches S_{x2} / S_{x4} - S_{x3} are closed. However, in this process, it is observed that devices S_{x2} and S_{x4} switch unnecessarily to synthesize the zero state. So, although the output is correct, the modulation can be further improved by employing a modified

The resultant switching commands for a typical operating point of $M = 0.83$ are shown in Figure 5-5. In Figure 5-3, the input command is compared with a threshold to determine IGCT switching. These switching events are passed through the sequential logic circuitry to obtain the IGCT switching signals with minimal switching. Simultaneously, the error between the command and IGCT output is given to the PWM block to determine IGBT switchings, according to the principles of the unipolar PWM.

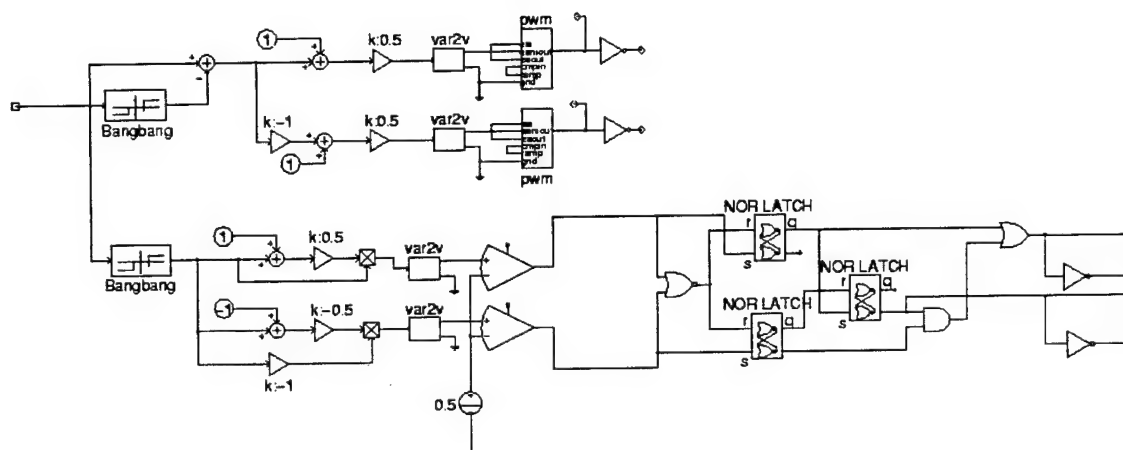


Figure 5-4. Circuit schematic of a sequential logic to ensure minimal switching.

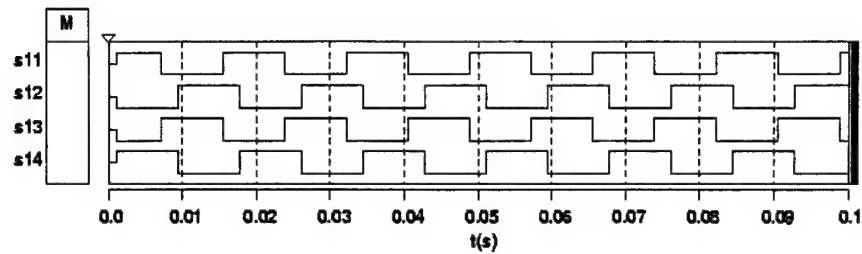


Figure 5-5. Modulating signals for individual devices with minimal switching.

5.3 Simulation Results

5.3.1 Hybrid Multilevel Inverters Simulations

Figure 5-6 through Figure 5-11 illustrate the representative voltages and currents of the hybrid multilevel inverter and the component inverters at modulation depths of 10%, 30% and 90%.

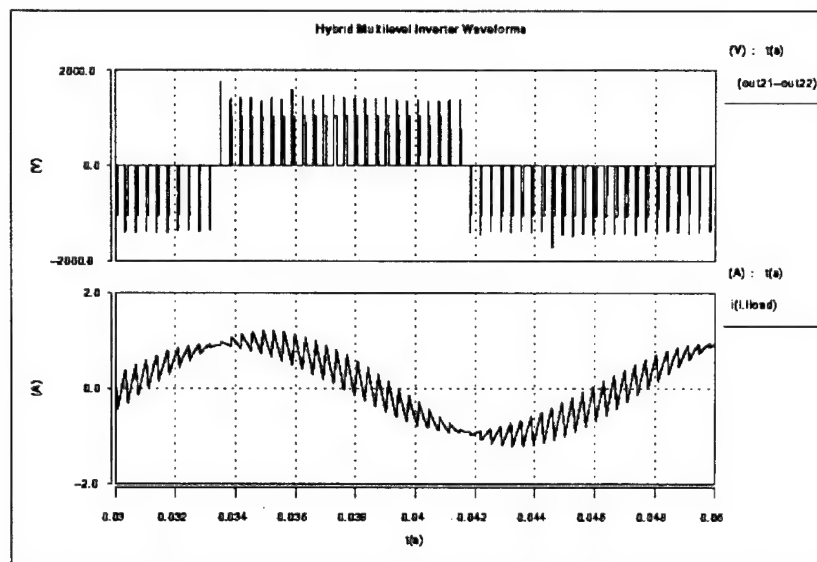


Figure 5-6. Hybrid multilevel inverter waveforms at $M = 10\%$.

Trace 1: Phase leg voltage, Trace 2: Load current.

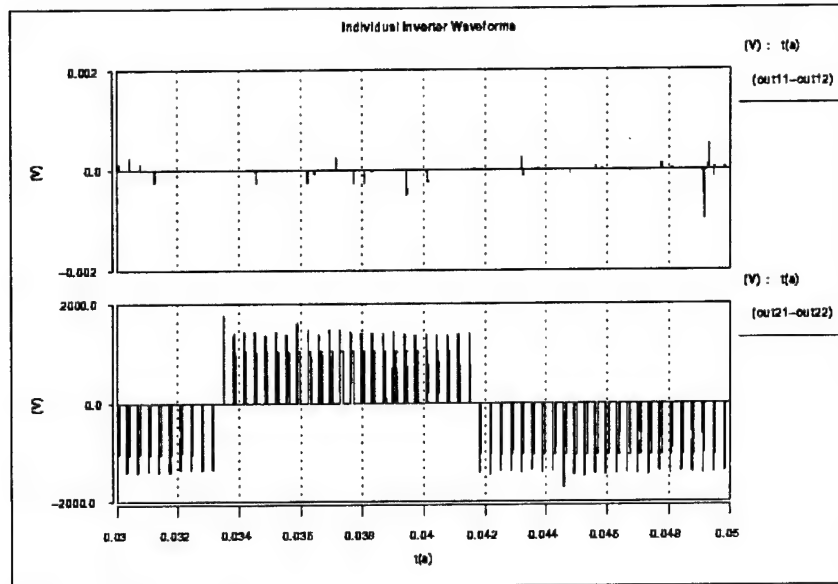


Figure 5-7. Individual inverter waveforms at $M = 10\%$.

Trace 1: IGCT inverter voltage, Trace 2: IGBT inverter voltage

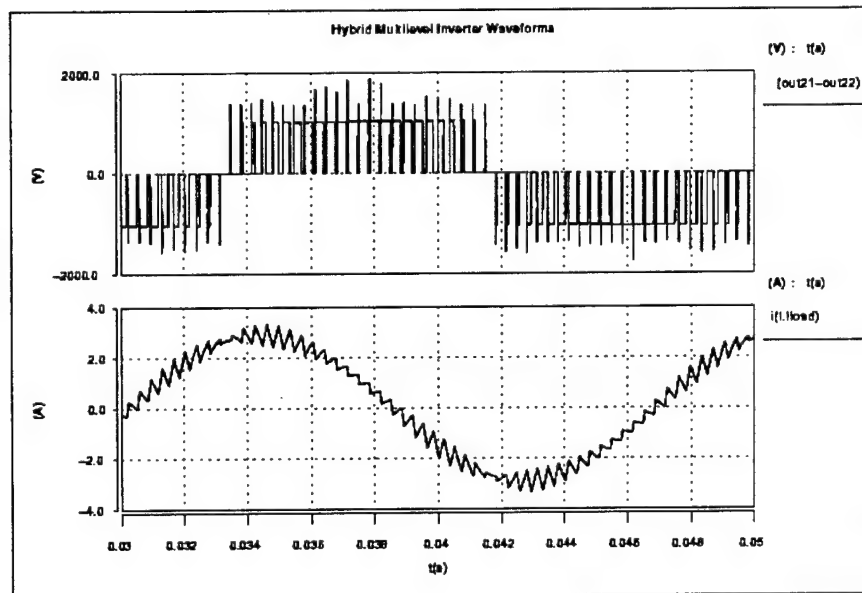


Figure 5-8. Hybrid multilevel inverter waveforms at $M = 30\%$.

Trace 1: Phase leg voltage, Trace 2: Load current.

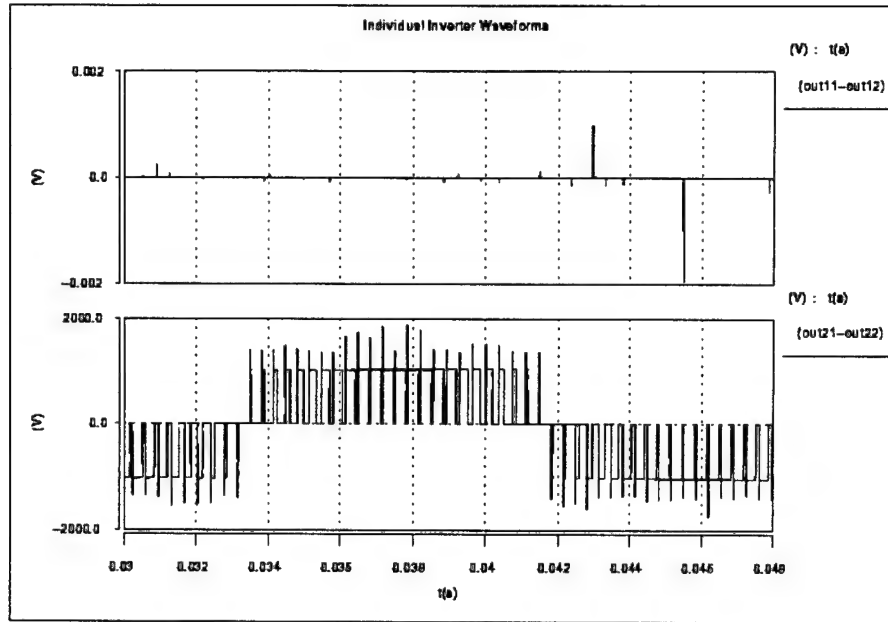


Figure 5-9. Individual inverter waveforms at $M = 30\%$.

Trace 1: IGCT inverter voltage, Trace 2: IGBT inverter voltage.

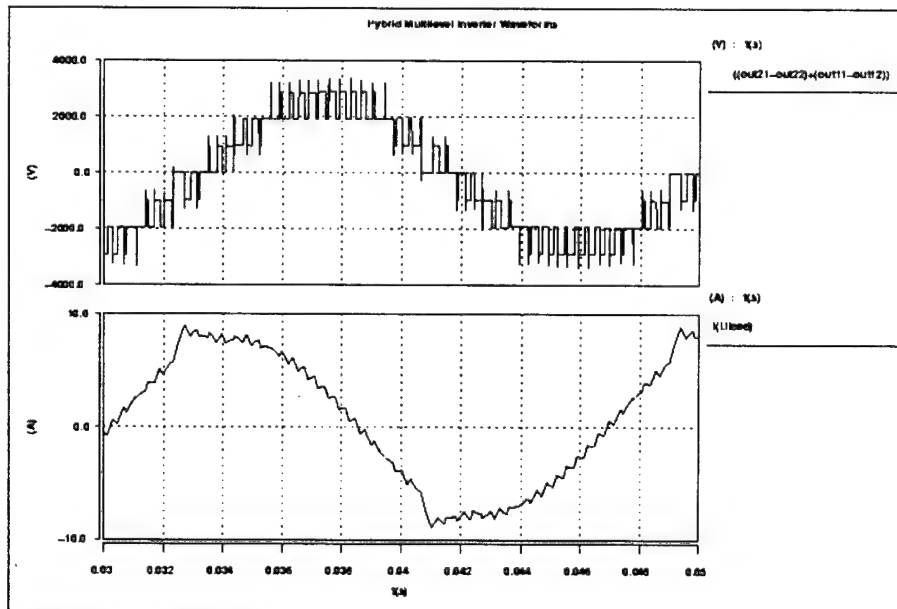


Figure 5-10. Hybrid multilevel inverter waveforms at $M = 30\%$.

Trace 1: Phase leg voltage, Trace 2: Load current .

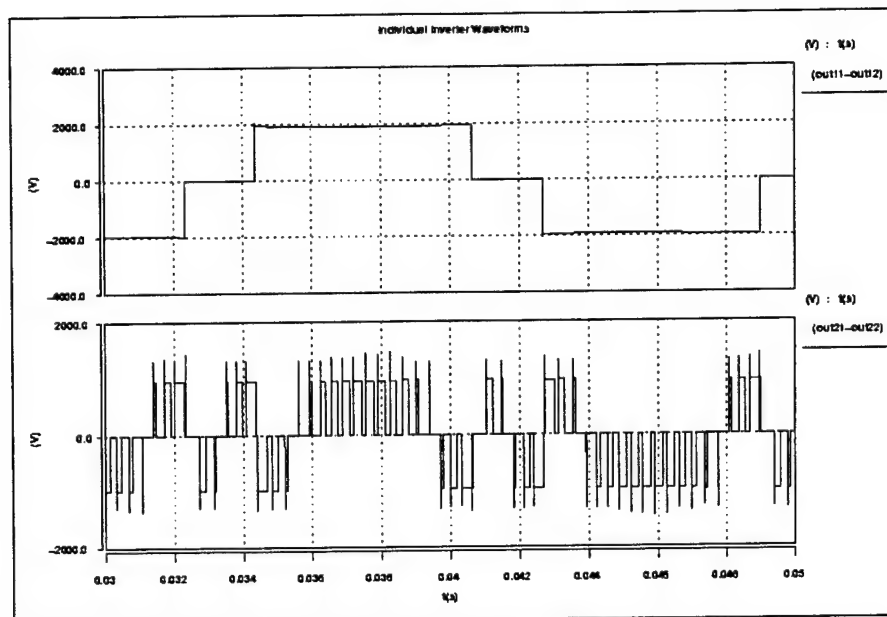


Figure 5-11. Individual inverter waveforms at $M = 90\%$.

Trace 1: IGCT inverter voltage, Trace 2: IGBT inverter voltage.

5.3.2 Simulation Results at $M = 0.83$ for Comparison

Detailed simulation results are presented for a modulation depth of $M = 0.83$. Figure 5-12 and Figure 5-13 illustrate the transient charging process in utility currents and DC link voltages. The hybrid multilevel inverter voltage and load current are shown in Figure 5-14. Figure 5-15 shows the component inverter voltages. The frequency spectra of these waveforms are illustrated in Figure 5-16 and Figure 5-17.

5.4 Conclusions

A circuit simulation model of a real hybrid multilevel inverter has been developed. Simulation results for various values of modulation depth M have been presented in detail, where inverter output voltages and spectra, DC bus voltages and the utility side currents are examined for both IGCT and IGBT inverters. The simulation results presented in this chapter will be verified through the experimental results in the following chapter.

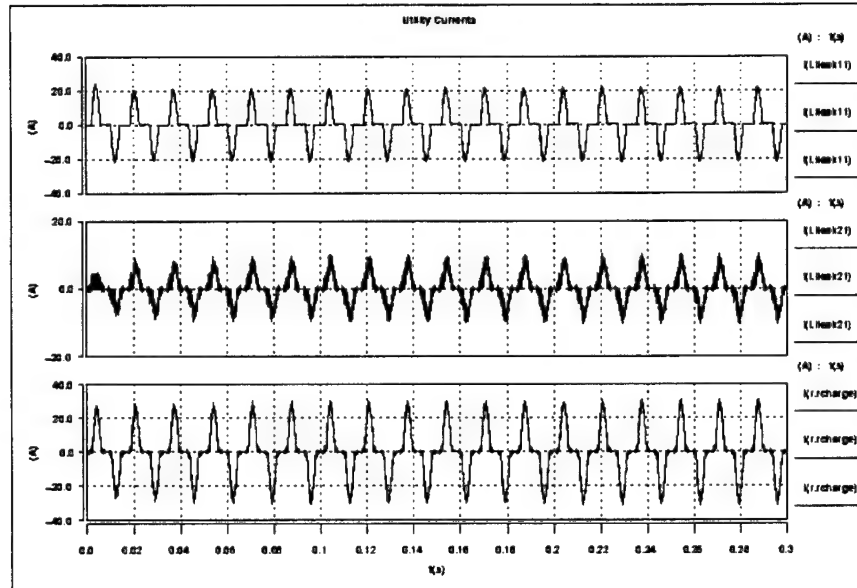


Figure 5-12. AC side (utility) charging currents.
Trace 1: High-voltage converter input current,
Trace 2: Low-voltage converter input current.

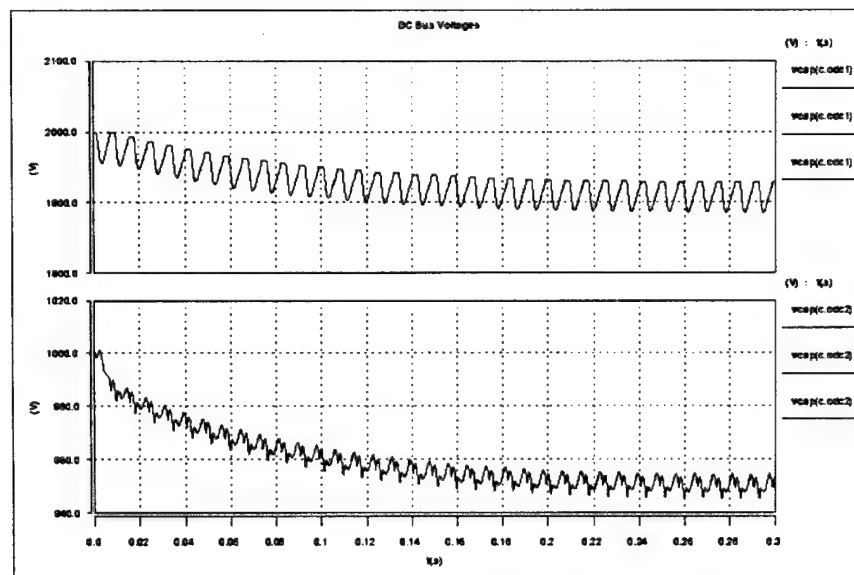


Figure 5-13. DC bus voltages.
Trace 1: High-voltage converter DC bus voltage,
Trace 2: Low-voltage converter DC bus voltage,
Trace 3: Total utility current.

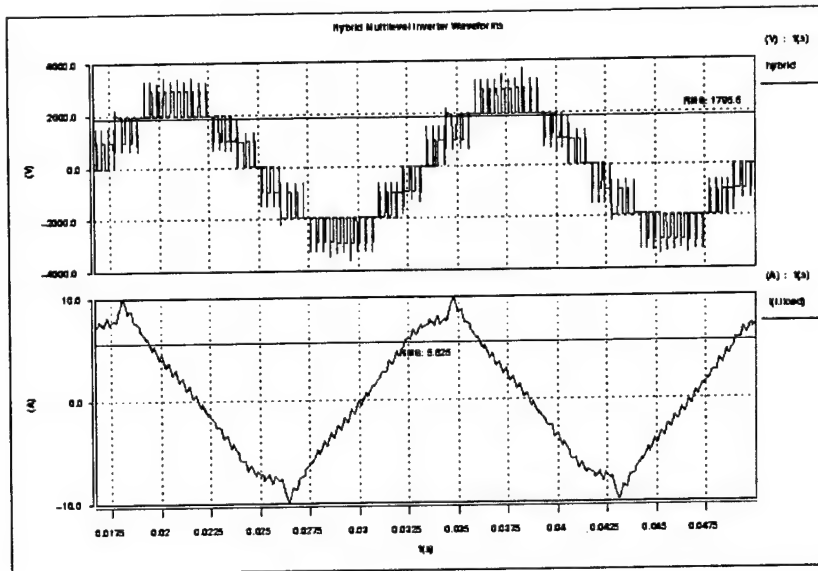


Figure 5-14. Hybrid multilevel inverter waveforms at $M = 0.83$.

Trace 1: Phase leg voltage, Trace 2: Load current.

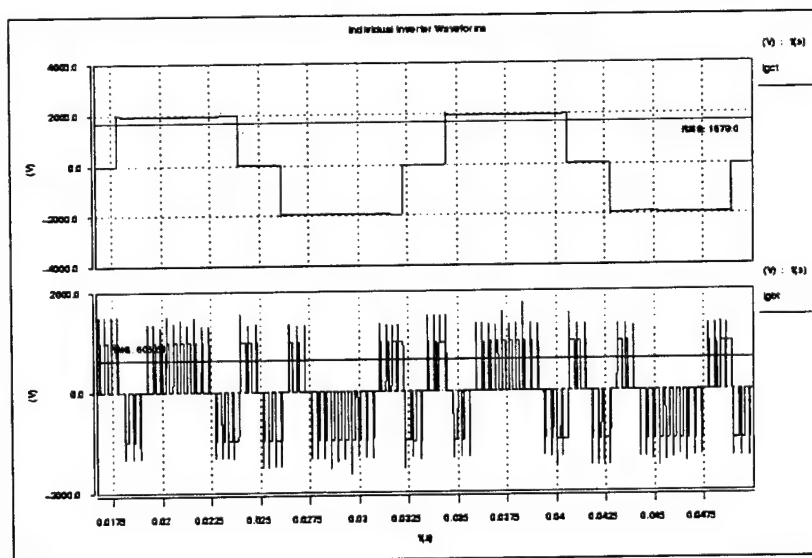


Figure 5-15. Individual inverter waveforms at $M = 0.83$.

Trace 1: IGCT inverter voltage, Trace 2: IGBT inverter voltage.

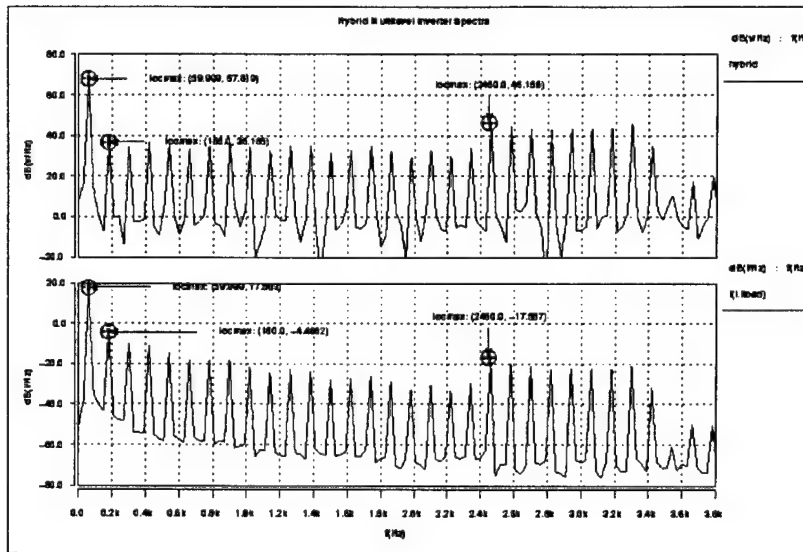


Figure 5-16. Hybrid multilevel inverter spectra at $M = 0.83$.

Trace 1: Phase leg voltage, Trace 2: Load current.

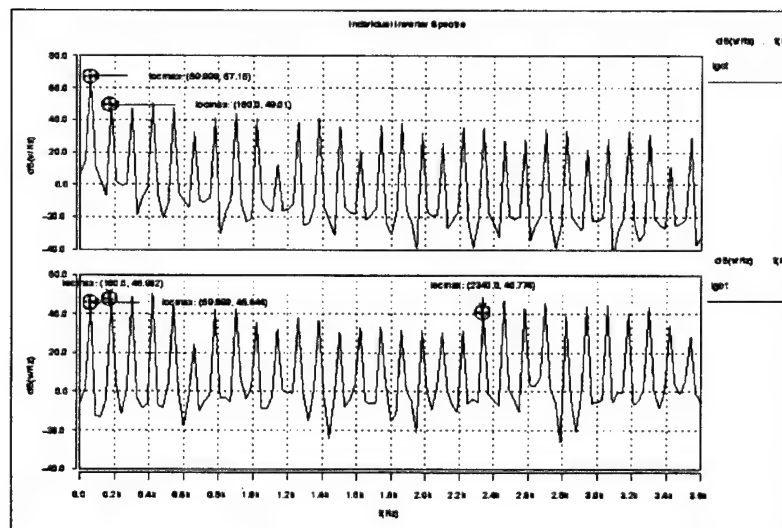


Figure 5-17. Individual inverter spectra at $M = 0.83$.

Trace 1: IGCT inverter voltage, Trace 2: IGBT inverter voltage.

Chapter 6 Hardware Prototype of the Hybrid Multilevel Inverter Including DSP Based Controller and Experimental Results

6.1 Introduction

This chapter describes the hardware prototype of a single leg of the seven-level hybrid inverter including the DSP-based controller. The system is supplied from a net DC voltage bus of 3300 V. As mentioned in earlier chapters, the DC bus is split in a 2:1 ratio, and the corresponding two H-bridge modules are built using IGCTs and IGBTs. The following section presents a top-down approach to system design. It includes a functional description of the entire system and functional partitioning of individual blocks. Section 4.3 discusses the electronic design procedure in detail and describes the circuit schematics for individual blocks. The industrial design elements are documented in Section 4.4. Finally, the experimental results are presented in Section 4.5.

6.2 System Configuration

6.2.1 Functional Description

The hybrid multilevel inverter system under investigation can be explained briefly with the help of a functional diagram presented in Figure 6-1. The system is fed by a 480 V supply derived from a three phase 480 V, 100 A power source. The supply line is passed through a variety of protection elements such as a circuit breaker, fuses and a metal oxide varistor (MOV). This is followed by a charge-up resistor, which can be bypassed with a relay that detects a DC bus charge-up. The 480 V line is then given to the isolation transformers, which also step it up to 1000 V and 2000 V respectively. The 1000 V supply is taken to the low-voltage power converter, which is comprised of back-to-back connected single-phase IGBT inverters with an intermediate DC link. The gates of the IGBT switches on the rectifier side are thereby shorted, using only the antiparallel diodes for passive rectification. The 2000 V line is taken to the high-voltage passive rectifier, which is built with discrete diodes. The rectified voltage is then filtered with a DC link capacitor and inverted via the single-phase IGCT inverter. Necessary snubber elements are included in the high-voltage rectifier and inverter stacks. The inverted AC outputs

from both the converters are combined and given to the load. One terminal of the low-voltage AC output is grounded in order to prevent any excessive voltages caused by floating terminals. The IGBTs are driven through a gate drive board, which is essentially built around an application specific integrated circuit (ASIC). The details will be presented in Section 9.3. The control signals to this ASIC are given by a digital signal processor (DSP) via an optical interface and blanking circuit. The DSP is the heart of the system and is controlled through a personal computer (PC). The ASIC requires an auxiliary power supply, which isolates and reflects it to the high-power side. The IGCTs are driven by the gate drive board, which are integrated with the device. The control signals for this gate drive are given directly from the DSP via optical interface and blanking circuitry. The auxiliary supply needed for the IGCT gate boards is also required to provide the necessary isolation. This supply is in turn fed through a regulated DC power supply. The fault protection schemes are based on overvoltage and overcurrent detection. Several current sensors are used in the system (along with two DC bus voltage detectors) to monitor the status of the system. These, in addition to the IGBT desat protection circuit, form the inputs to the fault protection board. The main circuit breaker is tripped in an event of a fault. In addition to the fault detection, the DC bus voltages are also monitored for the charge-up detection to be used to bypass the charge-up resistor.

6.2.2 Functional Partitioning

The system described in the previous subsection can be modularized into following eight functional blocks: power input elements, isolation and voltage transformation, high-voltage power converter, low-voltage power converter, load, controller element, fault/charge-up detection and protection elements and auxiliary power supplies.

6.2.2.1 Power Input Elements

Figure 6-2 illustrates the power input elements used in the system. These elements can be grouped as protection elements and charging elements. The protection elements are the circuit breaker (CB_{fault}), fuses (F_1 , F_2) and MOV. The charging elements are a charge-up resistor (R_{ch}) and a bypass relay (CB_{ch}). The power input and output for this module is

the single-phase 480 V line. In addition, live 110V control lines for two circuit breakers are used,, which get activated upon fault and charge-up detection.

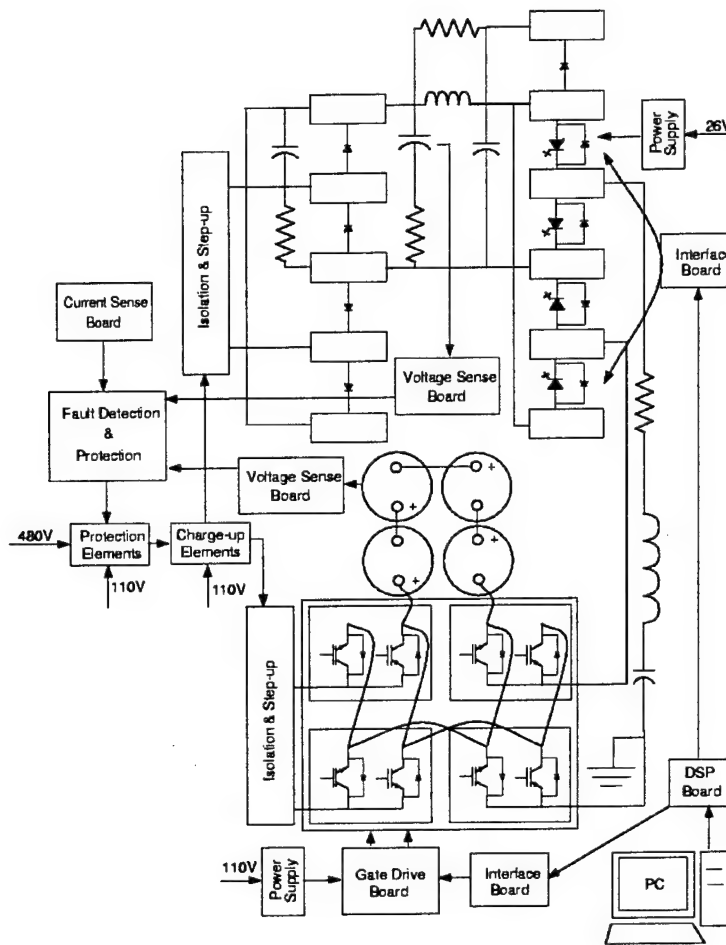


Figure 6-1. Functional diagram of the prototype inverter system.

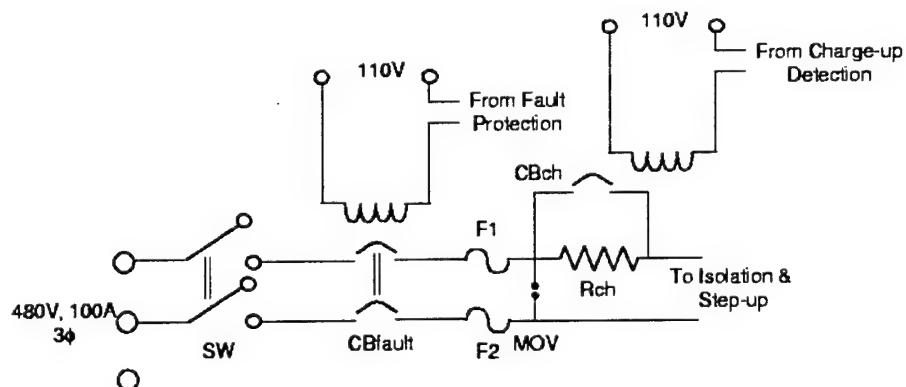


Figure 6-2. Schematic of the power input elements.

6.2.2.2 Isolation and Voltage Transformation

Figure 6-3 shows the schematics of the isolation and step up transformers used in the system. These transformers step up the 480 V supply to 1000 V (T_2) and 2000 V (T_1).

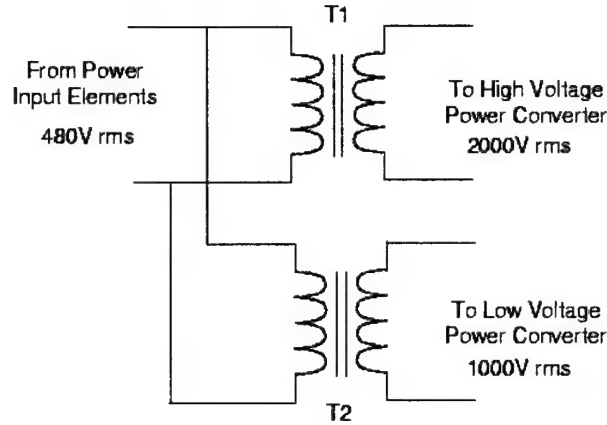


Figure 6-3. Schematic of the isolation and step-up transformers.

6.2.2.3 High-voltage Power Converter

The high-voltage power converter is shown in Figure 6-4. Structurally, it can be further modularized into rectifier stack, DC link and inverter stack. The rectifier stack consists of four diodes (SR_{11} - SR_{14}) and the corresponding R-C snubber (R_{sac} - C_{sac}). The DC link includes an oil-filled capacitor (C_{dc1}) with a series connected resistor (R_{dc1}). Although this resistor degrades the filtering performance, it will be able to limit the fault current in case of a DC link short-circuit fault. The capacitor and resistor are also shunted with a bleeding resistor (not shown), which bleeds off the charge when the system is not in operation. The inverter stack consists of four IGCTs (S_{11} - S_{14}) and a snubber diode (D_s). The rest of the snubber elements (inductor L_{sdc} , capacitor C_{sdc} and resistor R_{sdc}) are mounted on the stack. The power input to the high-voltage converter is a 2000 V line, while the output is a 2200 V quasi-square wave, the width of, which is depending on the operating point. The control lines to the IGCTs are optical and are supplied by the DSP via optical interface and blanking circuit. The four power supply lines to the gates are fed by one of the auxiliary power supplies.

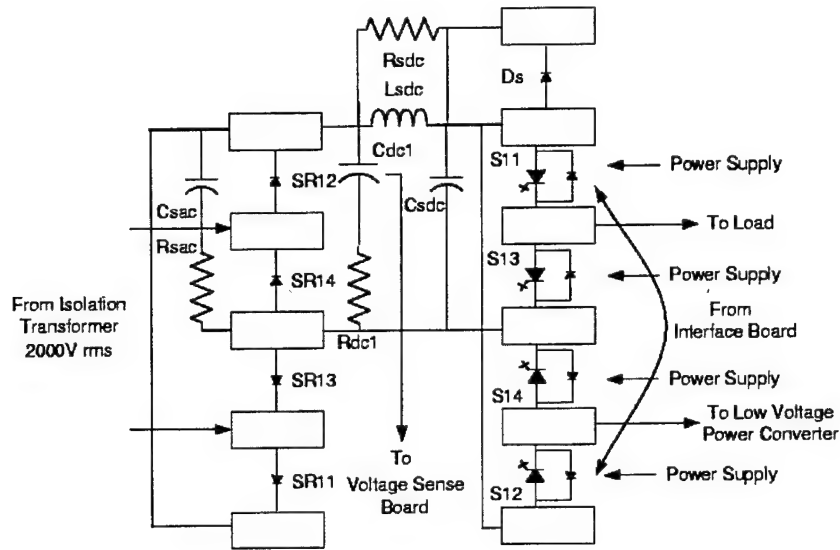


Figure 6-4. Schematic of the high-voltage power converter.

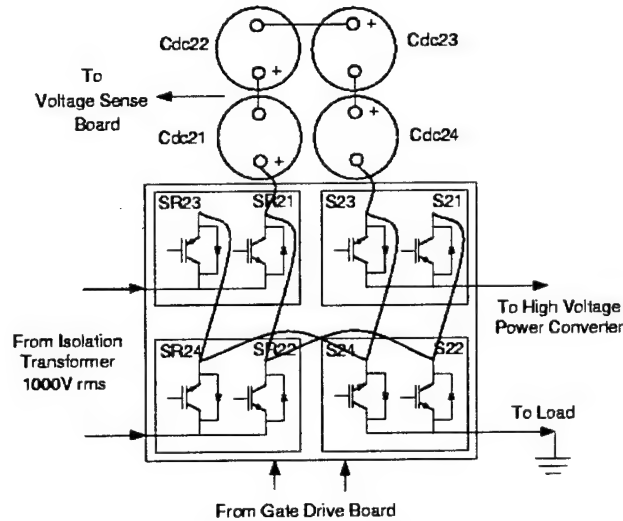


Figure 6-5. Schematic of the low-voltage power converter.

6.2.2.4 Low-voltage Power Converter

The low-voltage power converter is shown in Figure 6-5. Basically, it can be further modularized into device assembly and DC link. The device assembly consists of four modules, each having two devices (SR₂₁-SR₂₄ and S₂₁-S₂₄). As mentioned earlier, the gate leads of the devices on the rectifier side (SR₂₁-SR₂₄) are shorted, so as to operate in a passive mode. The DC link is composed of four capacitors (C_{dc21}-C_{dc24}) connected in a series on a laminar bus structure. The laminar bus structure is essential in order to reduce the bus inductance, which leads to undesirable spikes at device switchings. The DC bus

capacitors are shunted with high-frequency capacitors (not shown) to reduce their equivalent series inductance (ESL) and with resistors (also not shown) to ensure equal voltage sharing. These balancing resistors also act as bleeding resistors. The power input to the low-voltage inverter is a 1000 V line, while the output is PWM waveform, which is a function of the modulation depth. The gate control signals for the inverter IGBTs are supplied through the gate drive board.

6.2.2.5 Load

Figure 6-6, a passive R-L-C load is used to test the system. The capacitor (C_{load}) acts as a machine back-emf, while the R_{load} - L_{load} combination acts as the machine stator resistance and transient inductance. As mentioned earlier, one end of the load is grounded to ensure well-defined voltages at all points in the system.

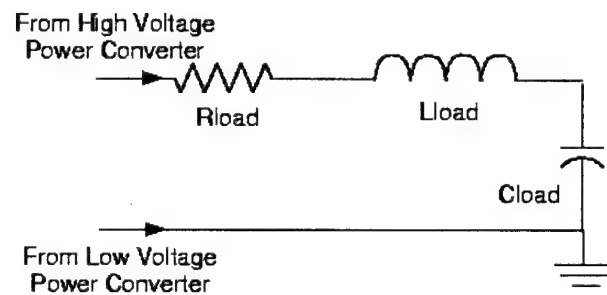


Figure 6-6. Schematic of the passive load.

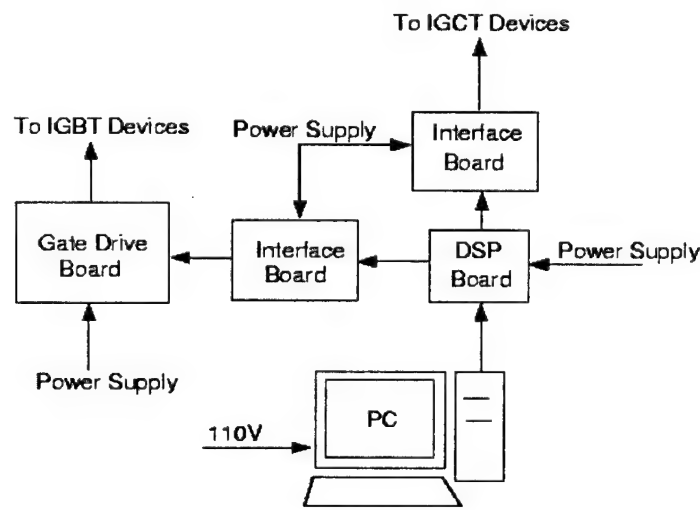


Figure 6-7. Controller elements block diagram.

6.2.2.6 Controller Elements

The controller elements can be classified as the PC, DSP board, blanking circuitry and optical interface (tied together in the interface board), and individual gate drives as depicted in Figure 6-7. The DSP is controlled by a PC via serial port interface. The DSP issues gate signals, which are passed through a blanking circuit to ensure that only one device is conducting in a leg at any given time. The signals are then converted to light outputs by optical interface circuit and then supplied to the individual gate drivers. The IGCT has a built-in gate drive. The IGBT gate drive is built around a ASIC dedicated to driving high-voltage IGBTs. The gate signals from the IGBT gate drive board are fed to the low-voltage power converter. The power required for the DSP, IGBT gate drive board and optical interface is derived from auxiliary power supplies.

6.2.2.7 Fault/Charge-up Detection and Protection Elements

Figure 6-8 shows the schematic arrangement of fault/charge-up detection and protection elements. Two types of faults, DC bus overvoltage and overcurrent, are to be detected. In order to do so, eight current sensors and two voltage sensors are used as shown. The current sensors are located as follows: The current sensors (4) in the IGBT converter legs detect a possible short-circuit if both the devices in the leg are conducting at the same time; the load and source current sensors (1 each) detect a short-circuit at the load and source side; finally, the current sensors on the transformer secondary side (2) detect a short-circuit at the secondary side of the transformers. The two DC bus voltages are measured to control the initial charging of DC buses before start up and detect a possible overvoltage. The current and voltage sensors feed the transduced signals, which, in addition to the IGBT desat protection circuit, form the inputs to the fault protection board. These inputs are checked for false alarm, and then transformed into a control action through logic circuits. The control signals from the fault/charge-up detection module are used to trip the main circuit breaker in case of a fault and operate the DC bus charge-up relay.

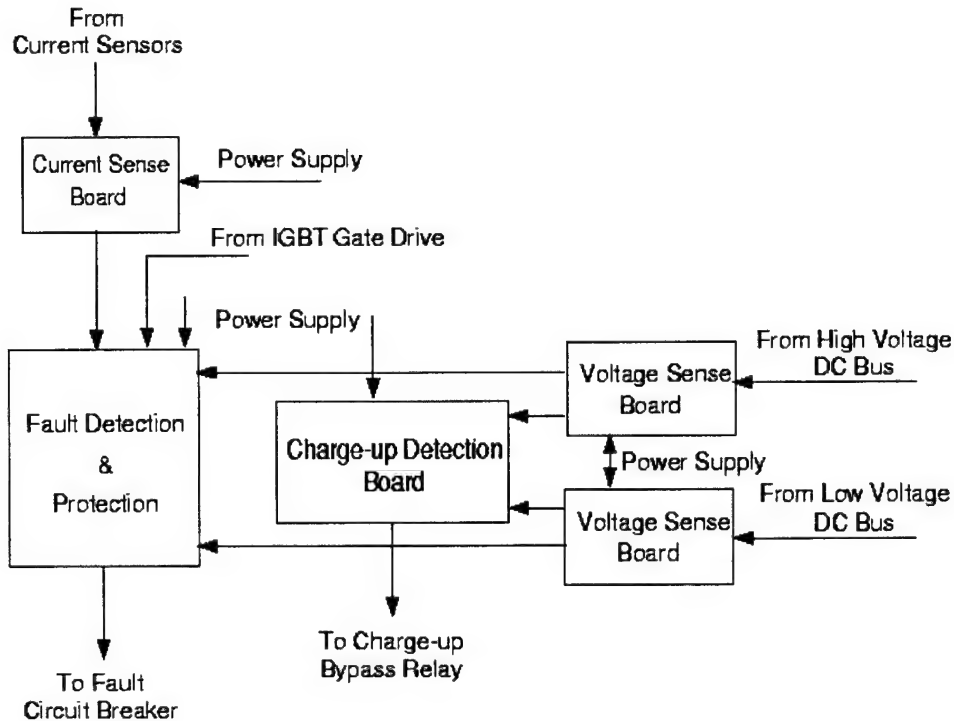


Figure 6-8. Fault/Charge-up detection and protection block diagram.

6.2.2.8 Auxiliary Power Supplies

Auxiliary power is needed for the DSP, sensing, logic and control circuitry and the gate drive boards. Regulated DC power sources are used (as shown in Figure 6-9) to supply power to these units. The power supply for the IGCT gate drives needs sufficient isolation and insulation breakdown margins (≥ 5 kV). Similar isolation is necessary for the DC voltage sense boards, which use differential voltage measurement. However, isolated power supplies are not needed for the low-voltage power converter, because the dedicated ASIC used for driving IGBTs provides the necessary isolation. Also, isolation is not necessary for the current sense boards because of the inherent galvanic isolation in electromagnetic current measurements.

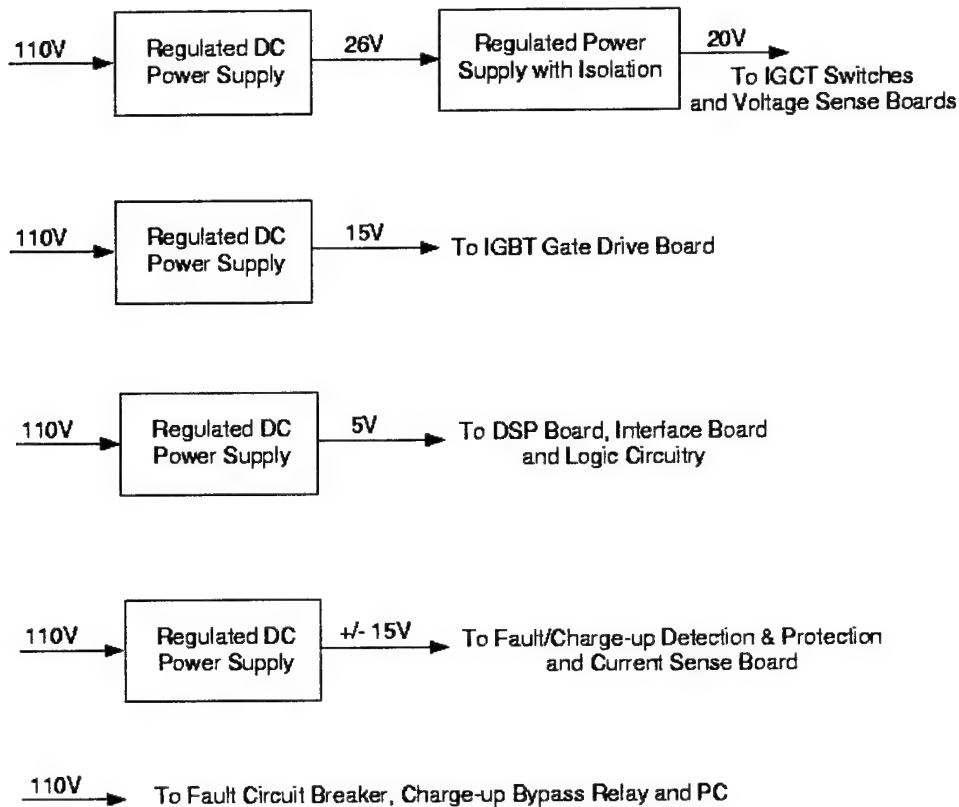


Figure 6-9. Auxiliary power supply block diagram.

6.2.3 Technical Specification

The electrical specifications of the designed prototype are shown in Table 1.

Table 9 Electrical specifications of the prototype inverter.

Parameter		
Input Voltage	480	V (rms)
Output Voltage	2400	V (rms)
Output Voltage	3300	V (peak)
Output Current	20	A (peak)
Output Power	25	kW
Input Frequency	60	Hz
Output Frequency	0-60	Hz
Total DC Voltage	3300	V
DC Voltage 1	2200	V
DC Voltage 2	1100	V
Switching Frequency 1	0-60	Hz
Switching Frequency 2	1440	Hz

6.3 Electronic Design

The elements from the eight functional blocks described in the previous section can be classified into the following four groups: main power elements, control elements, protection elements and auxiliary power supplies.

6.3.1 Main Power Elements

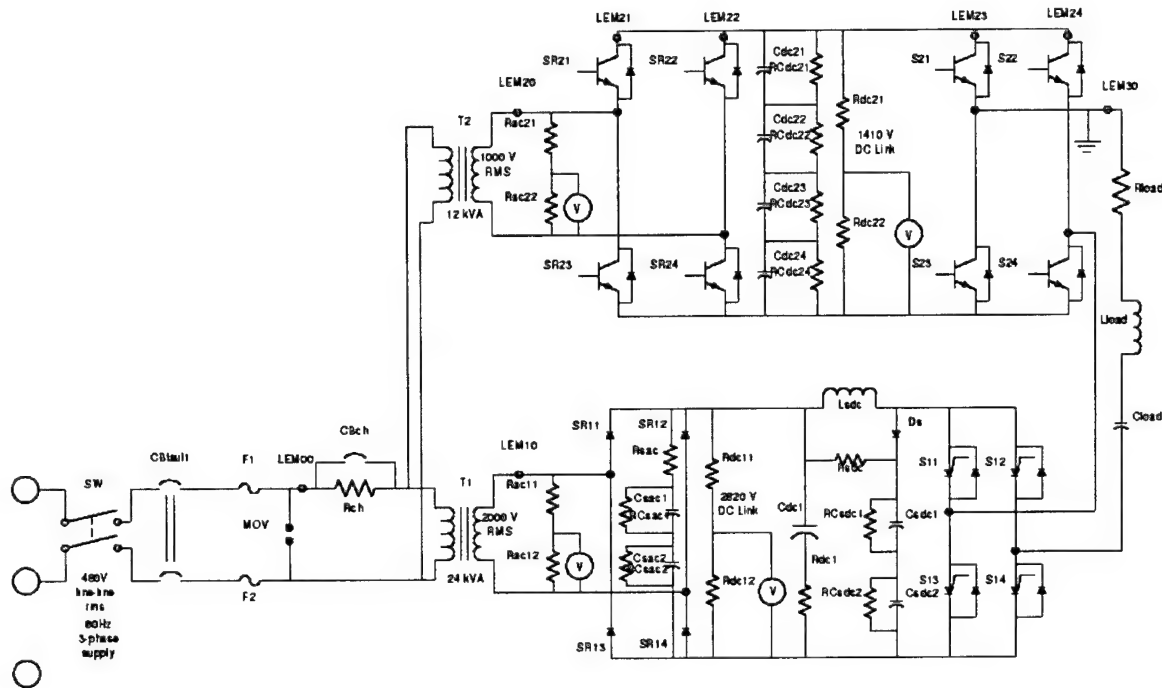


Figure 6-10. Circuit schematic of main power elements in the prototype system.

A circuit schematic of all the primary power elements used in the system is presented in . As mentioned earlier, the power source is a 480V supply. The power input elements, such as circuit breaker (CB_{fault}), fuses (F_1, F_2), MOV, charge-up resistor (R_{ch}) and by-pass relay (CB_{ch}) are used for protection and initial charging of the DC bus. The input current is monitored through the current sensor LEM00. The 480V supply is stepped up to 2000V and 1000V with two isolation transformers (T_1, T_2) with power ratings of 24kVA and 12kVA, respectively. The transformer's secondary currents are monitored using current sensors LEM10 and LEM20, while the voltages are displayed through voltage dividers built with resistors ($R_{\text{ac}11}, R_{\text{ac}12}, R_{\text{ac}21}, R_{\text{ac}22}$). The high-voltage (2000V) line is given to a passive rectifier bridge made up of diodes ($SR_{11}, SR_{12}, SR_{21}, SR_{22}$). An R-C snubber is used across the DC bus to prevent any undesirable voltage spikes during the reverse

recovery of diodes. The snubber resistor is denoted by R_{sac} , while the series connected snubber capacitors are denoted by C_{sac1} and C_{sac2} . Resistors RC_{sac1} and RC_{sac2} are used across the snubber capacitors to balance the voltages. A current limiting resistor (R_{dc1}) is connected with the DC link capacitor (C_{dc1}) to limit the current in event of a short-circuit fault. The high-voltage inverter is made up of four IGCTs (S_{11} , S_{12} , S_{21} , S_{22}). A snubber inductance (L_{sdc}) in the DC link limits the di/dt , which can trigger false operation of devices. Snubber diode (D_s) and capacitors C_{sdc1} and C_{sdc2} provide an alternative freewheeling path for the inductor current when the devices are opened. The resistors RC_{sdc1} and RC_{sdc2} prevent any voltage imbalance in the series-connected capacitors. The snubber capacitors are discharged into the DC link capacitor via a resistor R_{sdc} . The low-voltage (1000V) line is given to back-to-back connected single-phase IGBT bridges with an intermediate DC link. The IGBTs in the rectifier bridge are denoted as SR_{21} , SR_{22} , SR_{23} and SR_{24} while those in the inverter bridge are denoted as S_{21} , S_{22} , S_{23} and S_{24} . Current sensors LEM21, LEM22, LEM23 and LEM24 monitor the currents in each leg for fault detection. The DC link is composed of four capacitors (C_{dc21} , C_{dc22} , C_{dc23} and C_{dc24}) connected in series. Resistors RC_{dc21} , RC_{dc22} , RC_{dc23} and RC_{dc24} are used across them to balance the voltages. Both high and low DC link voltages are displayed through voltage divider circuits built with resistors R_{dc11} , R_{dc12} , R_{dc21} and R_{dc22} . The outputs of the two inverters are combined and given to load, which is composed of R_{load} , L_{load} and C_{load} . One end of the load is grounded. LEM30 is the sensor used to monitor load current.

6.3.2 Control Elements

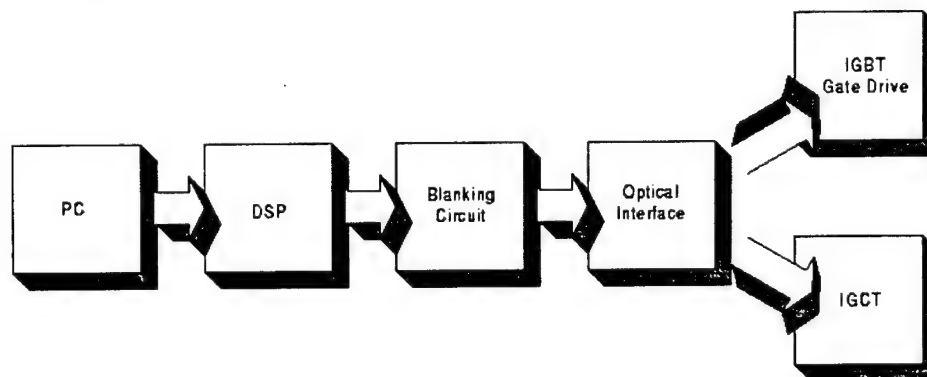


Figure 6-11. Block schematic of control elements in the prototype system.

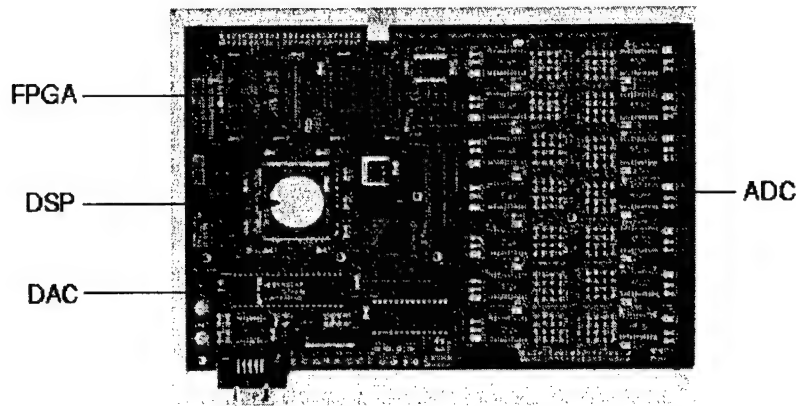


Figure 6-12. DSP board used in the prototype system.

A simplified block schematic of the control elements is shown in Figure 6-11. The control commands in the prototype are issued by a PC via a DSP. The inverter controller is built on a DSP board manufactured by CHS Engineering. The hardware is built around a processor from Analog Devices (ADSP21062). The processor has 32 MHz sampling frequency and an appreciable amount of built-in memory (2 Mbit) for the program and data. The DSP has been provided with the necessary peripherals for control applications: a fast A/D acquisition system, an FPGA-based numeric input/output system and a D/A converter. The system is completed with a memory for the permanent storage of data and a communication device. The board has 14 A/D converters with 12-bit resolution and 700 ns conversion time, which can be commanded simultaneously or individually. A D/A converter with four outputs and 10-bit resolution is also available on the DSP board. In addition, a XC4010PC84 FPGA manufactured by XILINX is used to execute standard routines, such as PWM. This PWM routine is used to generate control signals for the low-voltage IGBT inverter. A binary port in the DSP board is also available for the user. This has an 8-bit port and is used to control the switches in the high-voltage IGCT inverter. Figure 6-12 shows a picture of the DSP board.

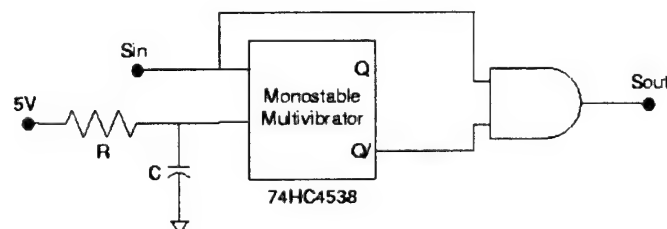


Figure 6-13. Blanking time generation block in the prototype.

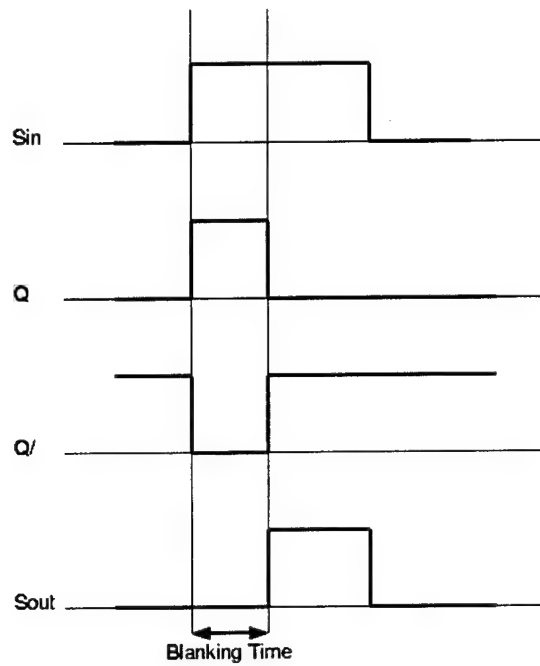


Figure 6-14. Blanking time generation timing chart.

To prevent simultaneous conduction of both the switches in a converter leg, a circuit to provide blanking time is necessary. A simplified schematic of such a circuit is shown in Figure 6-13. A given switch modulating signal S_{in} is delayed through a monostable multivibrator MC74HC4538, where the delay time is equal to the time constant of R-C network. The inverted delayed signal ANDed with the original signal gives the modified signal S_{out} with a blanking time. A typical timing diagram of the blanking time operation is shown in Figure 6-14. The blanking time is set for $10\mu s$ for both the IGCT and IGBT inverters. This circuit is used for all four legs in both the IGCT and IGBT inverters. Finally, the electrical signals with blanking time are converted into optical outputs with a fiber-optic transmitter HFBR1528.

6.3.3 Protection Elements

In a high-voltage setup like the proposed hybrid multilevel inverter system, it is necessary to devise fault detection and protection schemes carefully. A simplified schematic of the blocks used for fault and charge-up detection is shown in Figure 6-15.

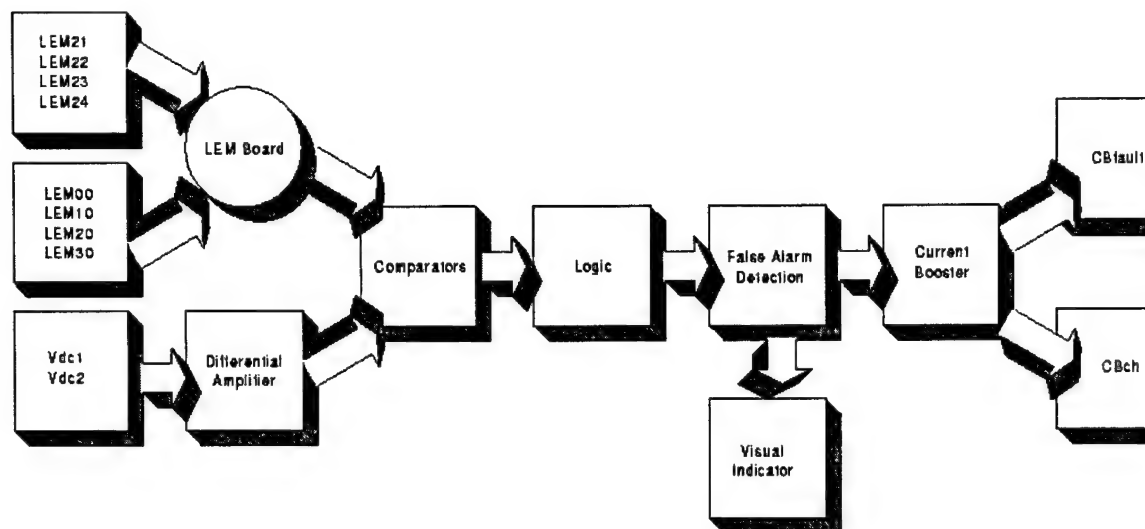


Figure 6-15. Fault protection and charge-up detection elements block diagram.

A fault can be classified as either an overcurrent fault or an overvoltage fault. The two DC bus voltages are monitored to detect an event of an overvoltage fault and also to monitor the charging of the DC bus. These voltages are measured using differential amplifiers. An overcurrent fault could be due to a short-circuit in the input source, load, either of the two DC links or at the transformer's secondary side. As shown in Figure 6-10, the current sensor modules LEM00, LEM30, LEM10 and LEM20 are used to detect an overcurrent at source, load or at transformer secondary sides. The desat protection algorithm in the IGBT gate drives detects a short-circuit fault in the IGBT converter structure. As an additional precaution, current sensors LEM21-LEM24 are installed to monitor currents in each IGBT converter leg. The values of currents obtained from the transducers are processed in the current sensor board.

A fault event is detected by comparing the real time values of the voltages and currents with a threshold. Upon fault detection, the main circuit breaker is opened, thereby disconnecting the power supply.

To prevent a spurious false fault signal from unnecessarily tripping the system, a false alarm detection circuitry is used. A simplified circuit diagram is shown in Figure 6-16.

Basically, this circuit introduces a time delaying R-C circuit before the fault signal is compared with the threshold level. To begin, let us assume a healthy operation,, which

implies that the output F_{out} is low. Since input F_{in} is also low, the output of the OR gate is low. Now, when a fault signal appears at F_{in} , it charges the R-C network. The time constant of the network is so adjusted that unless the fault input is high for 10 μ s, the output F of the R-C network doesn't reach the threshold level. This eliminates all the spurious false alarms, which usually last for less than 10 μ s. If a true fault is detected, the R-C network is charged up, which triggers the SR flip-flop to make $F_{out}=1$. This state is then eventually translated to opening of the main circuit breaker. Once the fault protection action is taken and the circuit breaker is open, the fault clears up, which causes the circuit breaker to close again. In order to prevent this, a feedback is used at the OR gate, which maintains the R-C networks level of charge. The fault status stays in this condition until the logic is manually acknowledged with the fault reset signal. This signal breaks the feedback loop and resets the flip-flop. The bleeding resistor used in shunt with the capacitor in the R-C network bleeds off the charge in the capacitor, thereby preventing unintentional tripping. The process of false alarm detection is summarized in Figure 6-17.

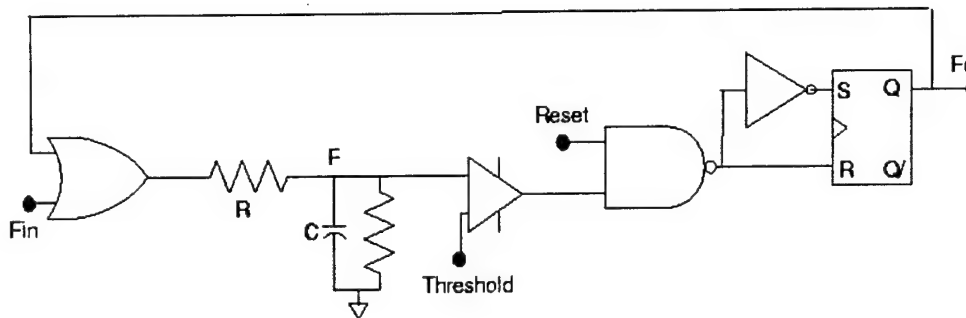


Figure 6-16. Schematic for false alarm detection in the prototype.

As explained in the previous sub-section, the IGBT gate drive used in this setup is built around IGD508E (data sheet in Appendix E), which has a built-in short-circuit protection. If an overcurrent would occur in the IGBT converter legs, the collector-emitter voltage is monitored to detect such a fault. When a device is in saturation region, this voltage is small and it increases as a function of the current carried by the device. Thus, an overcurrent condition would result in exceeding the nominal value of V_{CEsat} . In

such a condition, the gate drive IGD508E turns off the device and keeps it in blocked condition for a defined minimum amount of time,, which is set on the gate drive board. The gate drive also issues an indication of a fault event to the fault detection board, as depicted in Figure 6-8.

The fault detecting signals obtained through current sensors, voltage sensors and IGBT desat protection are combined in a logic circuit and confirmed for their validity in the false alarm detection block (Figure 6-15). Upon verifying their authenticity, they are passed to the current boosters, which operate the relays.

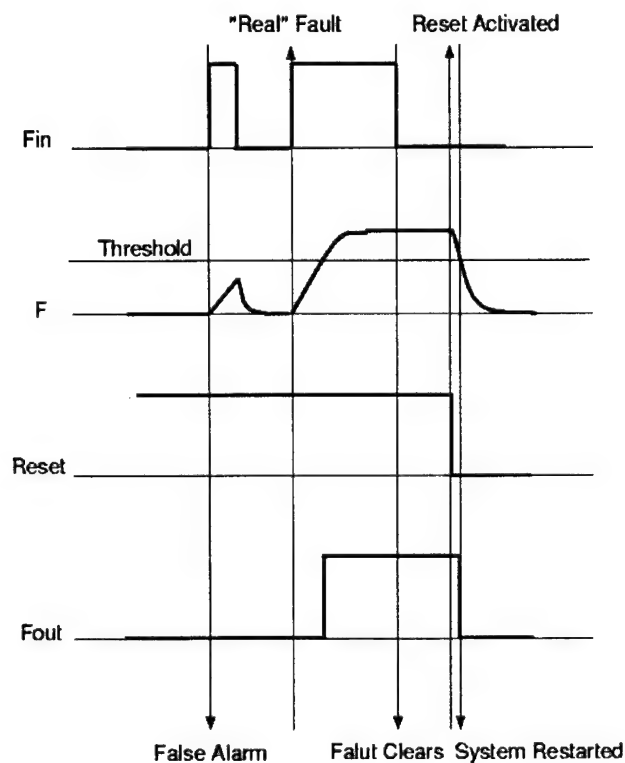


Figure 6-17. False alarm detection timing chart.

6.3.4 Auxiliary Power Supplies

Auxiliary power is needed for the DSP, sensing, logic and control circuitry and the gate drive boards. The IGCT gate drive boards and voltage detection boards need a supply with high isolation, so a commercial supply is used.

6.4 Experimental Results

The hybrid multilevel inverter is tested extensively at various modulation depths in the laboratory. This section presents selected experimental results obtained during the testing. All voltages are measured with high-voltage probes, and all currents are measured through current sensors installed in the system.

6.4.1 Charge-up Test

A soft-start circuit has been installed in the converter, as described in earlier sections. It consists of a simple resistor, which can be bypassed on detecting the voltages in DC links. This is to limit and damp the input inrush current at the start-up. Figure 6-18 shows the DC link voltages charging up from 0-1500V and 0-750V. When the DC bus capacitors are charging, the current flows through the charge-up resistor R_{ch} . When the charge-up thresholds are reached, the relay CB_{ch} closes, thereby creating an alternate path for the current. This is shown in Figure 6-19. A zoomed-in view of the same plots are shown in Figure 6-20 and Figure 6-21 for detailed inspection. It may be seen that the peak input current is limited to 35A.

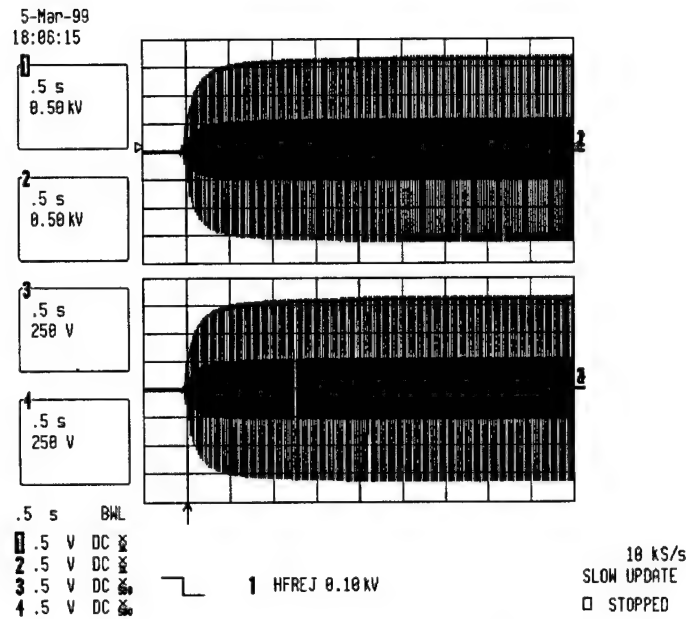


Figure 6-18. Measured voltages during DC bus charging.

Trace 1: IGCT DC bus voltage(500V/div);
Trace 2: High-voltage transformer secondary voltage (500V/div);
Trace 3: IGBT DC bus voltage(250V/div);
Trace 4: Low-voltage transformer secondary voltage (250V/div).

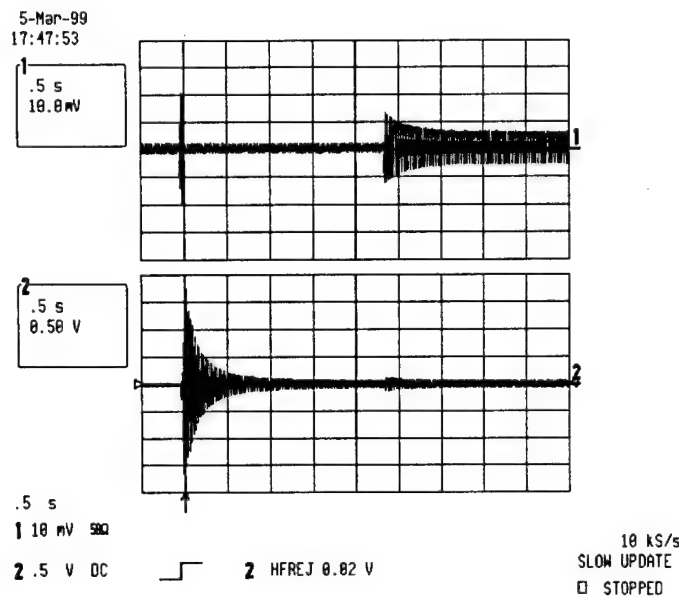


Figure 6-19. Measured currents during DC bus charging.

Trace 1: Current through charge-up relay (2A/div);
Trace 2: Input current (10A/div).

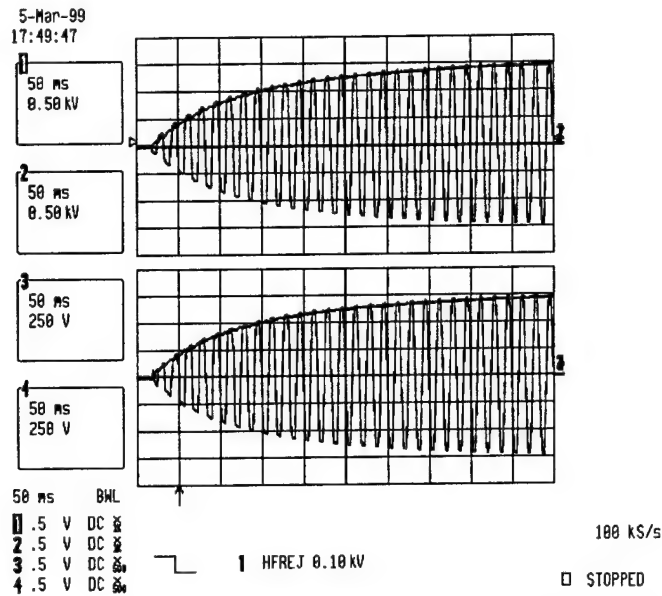


Figure 6-20. Measured (zoomed-in) voltages during DC bus charging.

Trace 1: IGCT DC bus voltage(500V/div);
Trace 2: High-voltage transformer secondary voltage (500V/div);
Trace 3: IGBT DC bus voltage(250V/div);
Trace 4: Low-voltage transformer secondary voltage (250V/div).

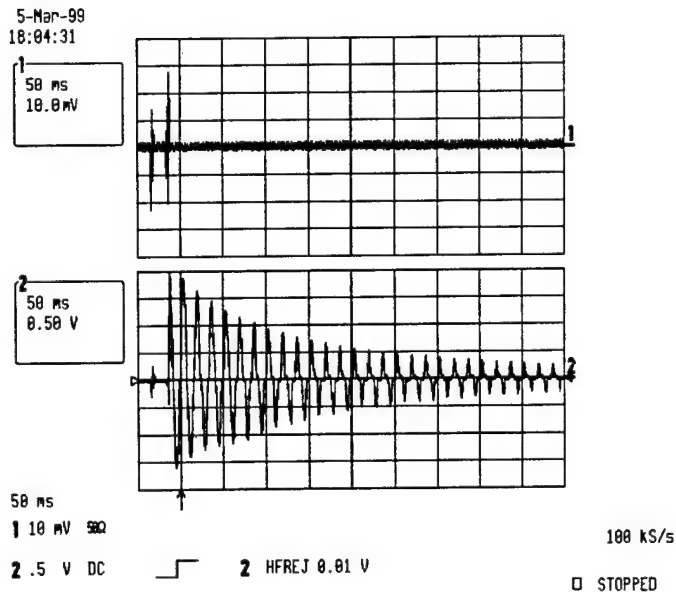


Figure 6-21. Measured (zoomed-in) currents during DC bus charging.

Trace 1: Current through charge-up relay (2A/div);
Trace 2: Input current (10A/div).

6.4.2 Initial Testing of Individual Inverters

Both high and low-voltage inverters are initially tested on a R-L ($R = 10\ \Omega$ and $L = 100\text{ mH}$) load. The IGCT inverter is modulated to give a quasi-square wave at 300 Hz, whereas the IGBT inverter is controlled in a unipolar PWM fashion at 1 kHz. The DC bus voltages for the high and low-voltage inverters are set at 1100V and 250V, respectively. Individual inverter operation waveforms are shown in Figure 6-22 and Figure 6-23.

6.4.3 Hybrid Multilevel Inverter Tests

Figure 6-24 through Figure 6-29 illustrate the output voltages and currents of the hybrid multilevel inverter and the component inverters at modulation depths of 10%, 30% and 90%. The IGCT inverter feeds the power back to the IGBT inverter in the central zone of modulation depths. Since there is no provision of regeneration in the IGBT inverter, this region is avoided in the experimental measurements.

6.4.4 Experimental Results at $M = 0.83$ for Comparison

The measured waveforms of the hybrid multilevel inverter and individual inverters at modulation depth $M = 0.83$ are shown in Figure 6-30 and Figure 6-31. They may be compared with the corresponding waveforms obtained via circuit simulations presented in the previous chapter. The frequency spectrum of the multilevel inverter, load current and the component inverters at this operating point are shown in Figure 6-32 through Figure 6-35, and may also be compared against the spectra presented in the previous chapter.

6.5 Conclusions

A working prototype of one leg of a hybrid seven-level inverter rated for 4.16 kV and 100 HP was constructed in the laboratory. This chapter documents the design methodology adopted to build this prototype. The prototype is tested at various operating points and experimental data is included in this chapter.

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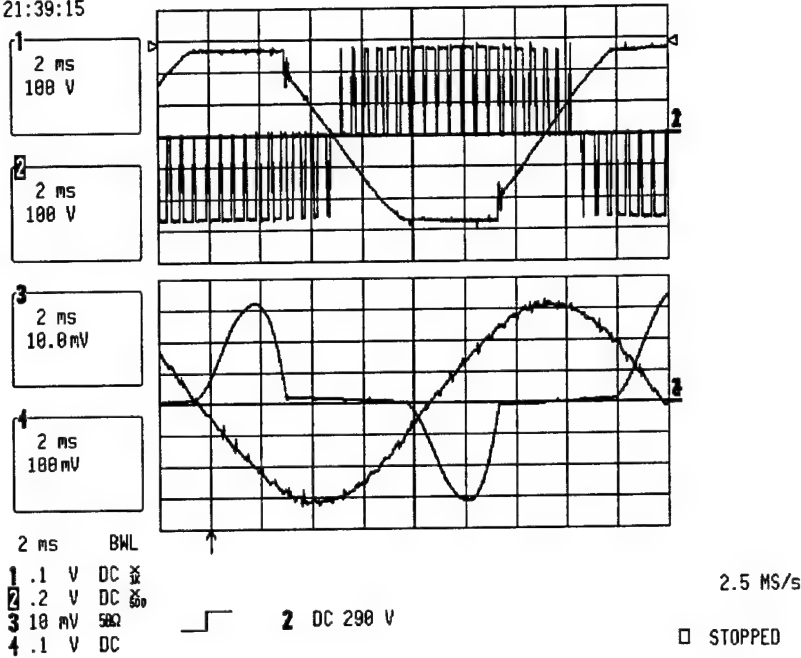


Figure 6-22. Measured voltages during IGCT inverter testing.

Trace 1: High-voltage transformer secondary voltage (500V/div);

Trace 2: IGCT inverter output voltage (500V/div);

Trace 3: Output current (2A/div); Trace 4: Input current (4A/div).

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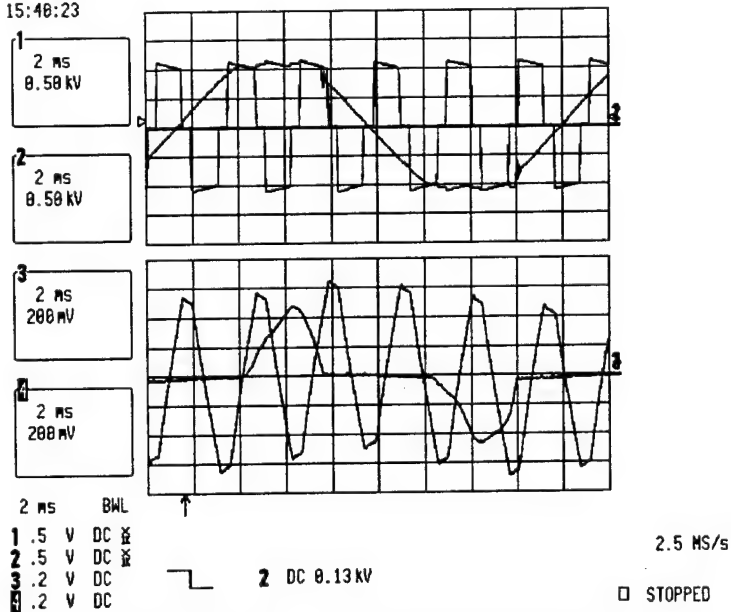


Figure 6-23. Measured voltages during IGBT inverter testing.

Trace 1: Low-voltage transformer secondary voltage (100V/div);

Trace 2: IGBT inverter output voltage (100V/div);

Trace 3: Output current (2A/div);

Trace 4: Input current (2A/div).

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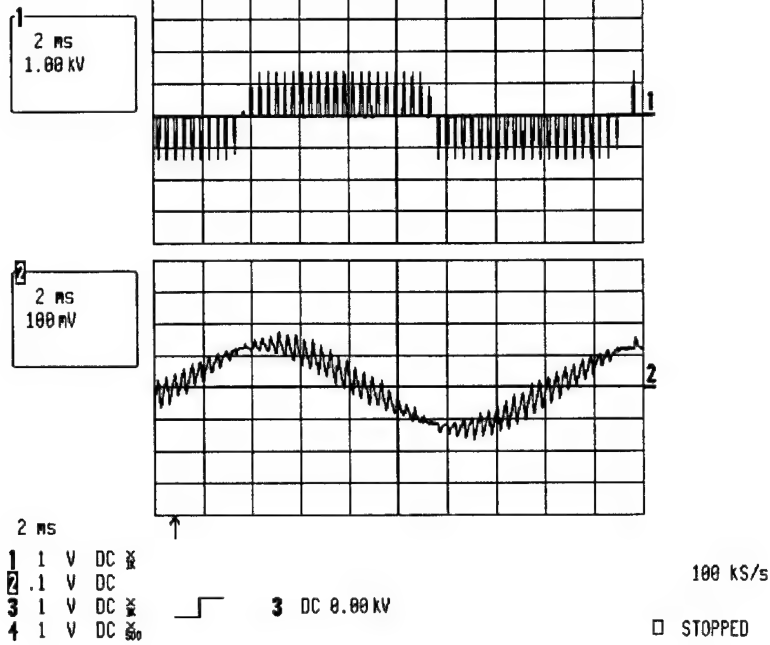


Figure 6-24. Hybrid multilevel inverter waveforms at $M = 10\%$.

Trace 1: Phase leg voltage (1000V/div);
Trace 2: Load current (1A/div).

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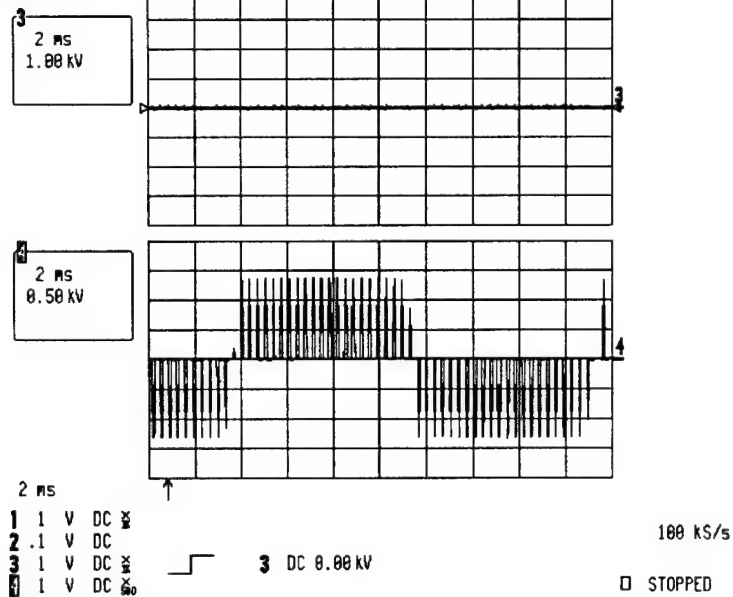


Figure 6-25. Individual inverter waveforms at $M = 10\%$.

Trace 1: IGCT inverter voltage (1000V/div), Trace 2: IGBT inverter voltage (500V/div).

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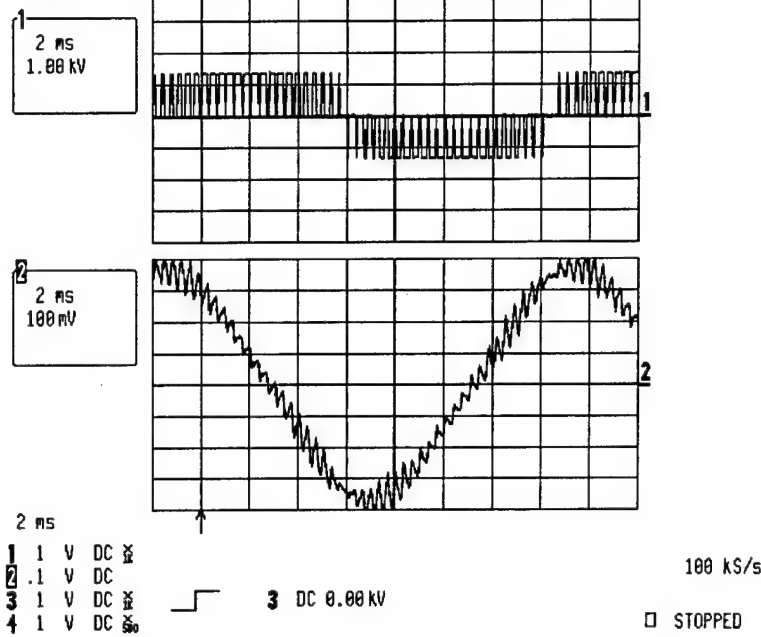


Figure 6-26. Hybrid multilevel inverter waveforms at $M = 30\%$.

Trace 1: Phase leg voltage (1000V/div), Trace 2: Load current (1A/div).

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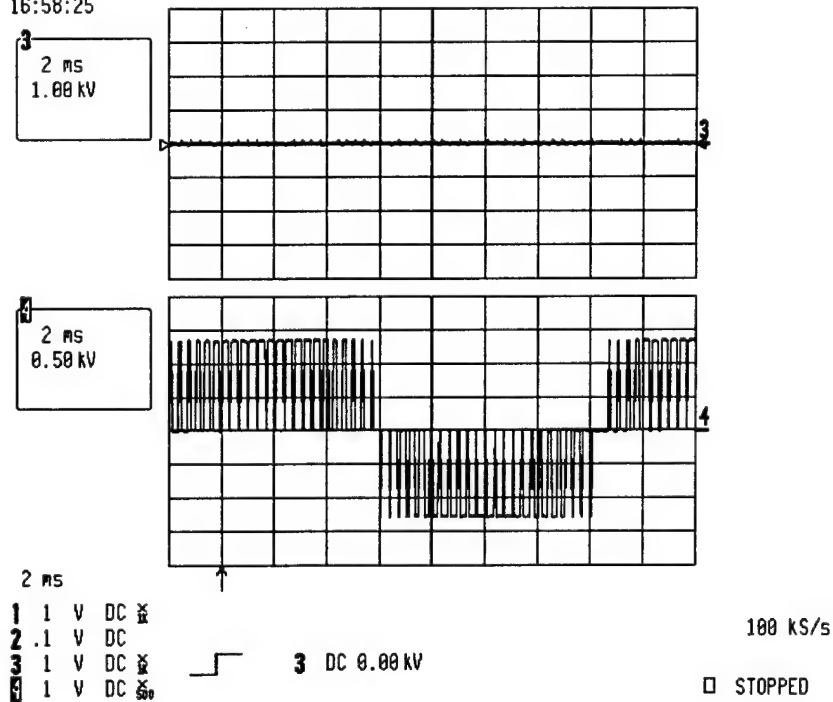


Figure 6-27. Individual inverter waveforms at $M = 30\%$.

Trace 1: IGCT inverter voltage (1000V/div), Trace 2: IGBT inverter voltage (500V/div).

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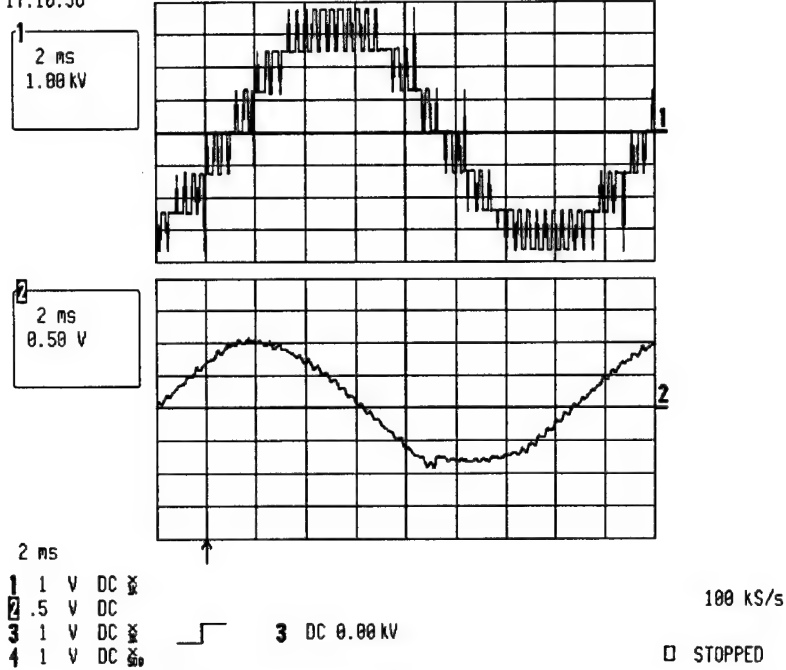


Figure 6-28. Hybrid multilevel inverter waveforms at $M = 90\%$.

Trace 1: Phase leg voltage (1000V/div), Trace 2: Load current (5A/div).

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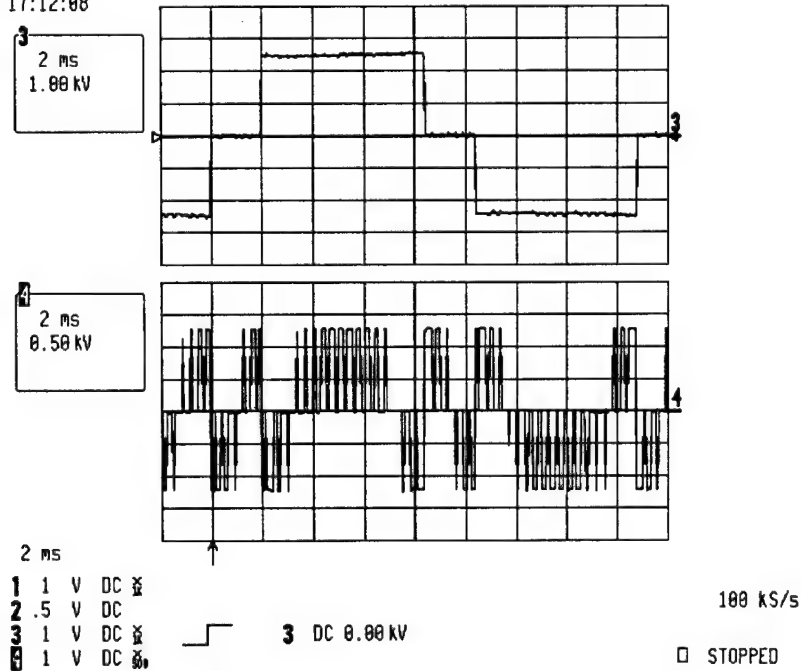


Figure 6-29. Individual inverter waveforms at $M = 90\%$,

Trace 1: IGCT inverter voltage(1000V/div), Trace 2: IGBT inverter voltage (500V/div).

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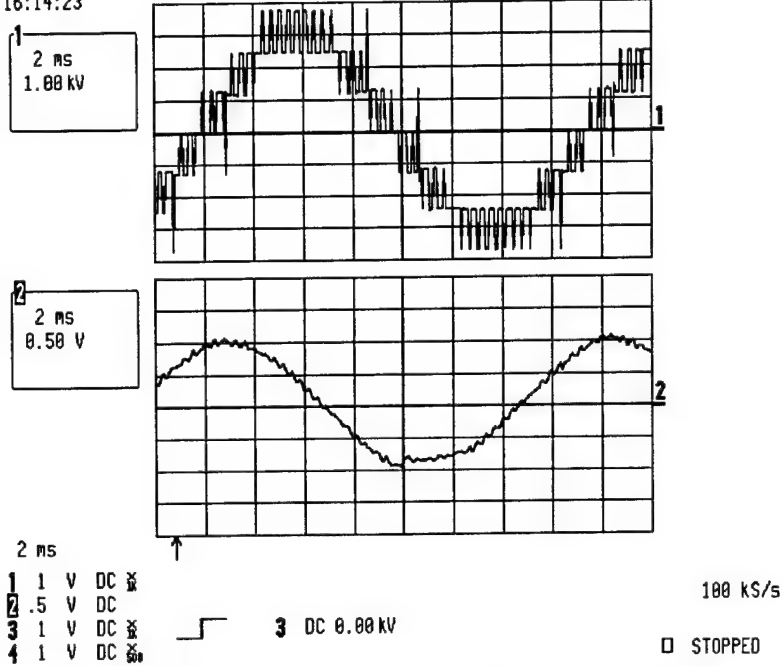


Figure 6-30. Hybrid multilevel inverter waveforms at $M = 0.83$.

Trace 1: Phase leg voltage (1000V/div), Trace 2: Load current (5A/div).

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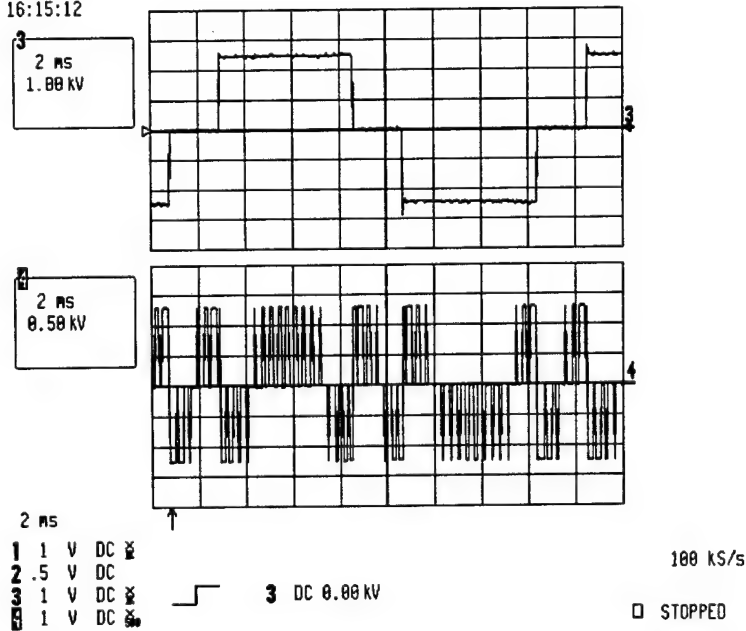


Figure 6-31. Individual inverter waveforms at $M = 0.83$.

Trace 1: IGCT inverter voltage (1000V/div);
Trace 2: IGBT inverter voltage (500V/div).

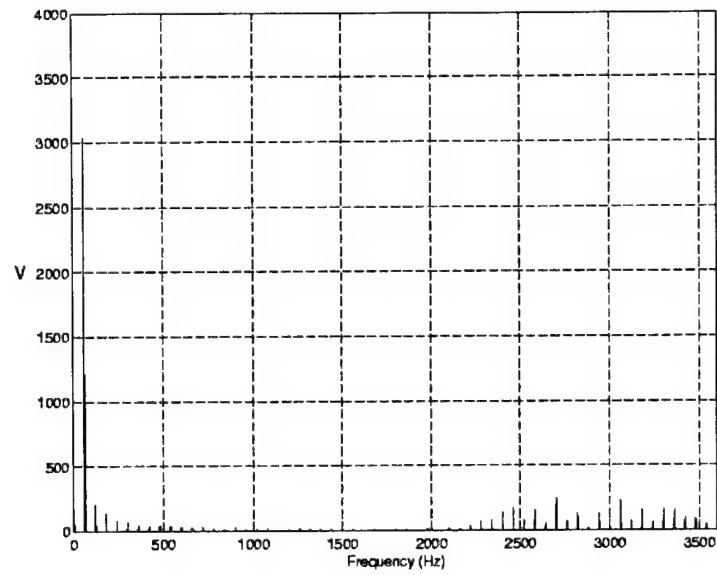


Figure 6-32. Frequency spectrum of the phase leg voltage.

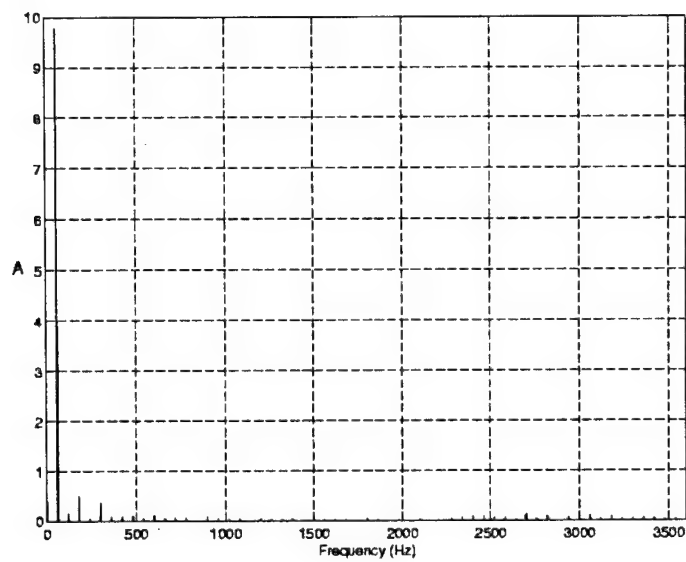


Figure 6-33. Frequency spectrum of the load current.

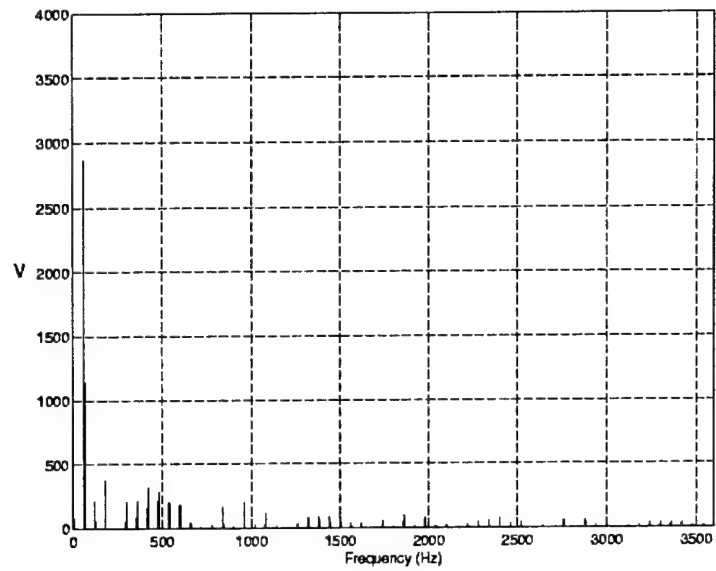


Figure 6-34. Frequency spectrum of the IGCT inverter voltage.

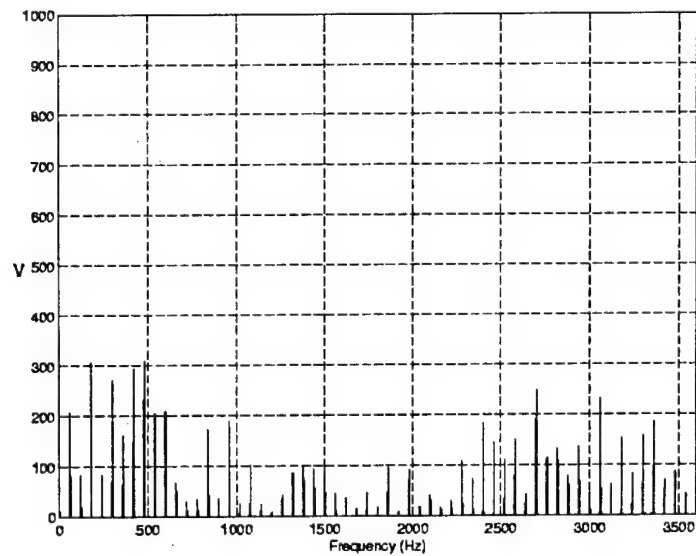


Figure 6-35. Frequency spectrum of the IGBT inverter voltage.

Chapter 7 Complementary Half Controlled Three Phase Rectifier

7.1 Introduction

A study on the half controlled three phase pulse width modulated (HC3 Φ PWM) boost rectifier has been reported in a recent publication [1]. This rectifier has simpler and more robust structure compared to the full controlled three phase (FC3 Φ) PWM boost rectifier (reduced switch count and shoot through free legs), and better performance compared to the diode rectifier (actively controlled dc link voltage and lower input current total harmonic distortion (THD)) [1]. One of the main drawbacks is its even harmonic input current distortion which may cause undesirable resonance problems [1], [2]. Other issues of concern are fairly large ac side inductance and the necessity of intentional lagging power factor current command to obtain reasonably low input current THD [1].

This paper describes methods with which the abovementioned problems can be handled for a certain type of applications by using complementarily configured HC3 Φ PWM boost rectifiers. These applications are those which need multiple dc links, e.g. H-bridge multilevel inverter systems [3] or some types of multidrive systems [4]. Therefore, one can expect to obtain modularized power conversion front-ends for multi dc link demands. This approach has a great potential as a candidate of the power electronics building block (PEBB) applications.

In the following sections, power stage description, control principles, simulation results and experimental results are presented. A conventional hysteresis current regulator is assumed as the method of current control throughout this work.

7.2 Complementary Half Controlled Three Phase PWM Boost Rectifiers

Figure 7-1 shows a power stage schematic of the complementary HC3 Φ PWM boost rectifier. The system consists of two HC3 Φ PWM boost rectifiers [1] configured in complementary manner combining one collector common and one emitter common topology. This can be called *the rectifier leg complementary* configuration.

In both of the emitter common and collector common HC Φ PWM boost rectifiers, it can be said that they have simpler structure compared to FC3 Φ PWM boost rectifiers (only three controlled switches and gate drives, shoot through free leg structure), and are capable of better performance compared to diode rectifiers (actively controlled dc link voltage and lower input current THD). In addition, for the emitter common HC3 Φ PWM boost rectifier, only one floating power supply for three gate drives is needed due to the emitter common structure. If complementary power semiconductor devices with comparable performance and cost would be available, a single floating power supply could be used for the collector common rectifier as well.

If the application needs input transformers for galvanic isolation, as in H-bridge multilevel inverters, the complementary structure can be transferred from the rectifier legs to the transformer secondary windings. Figure 7-2 shows a power stage schematic of this topology. This can be called *the input transformer complementary configuration*.

In the transformer complementary approach, only the emitter common half controlled bridge topology can be used as a common building block. In Figure 7-2, the ac side inductors, L_{ac} , can be thought of as partially or entirely leakage inductance of the input transformer.

It may be noted that the HC3 Φ PWM boost rectifiers do not have power regenerating capability. This is incurred at the cost of obtaining shoot through free leg structure.

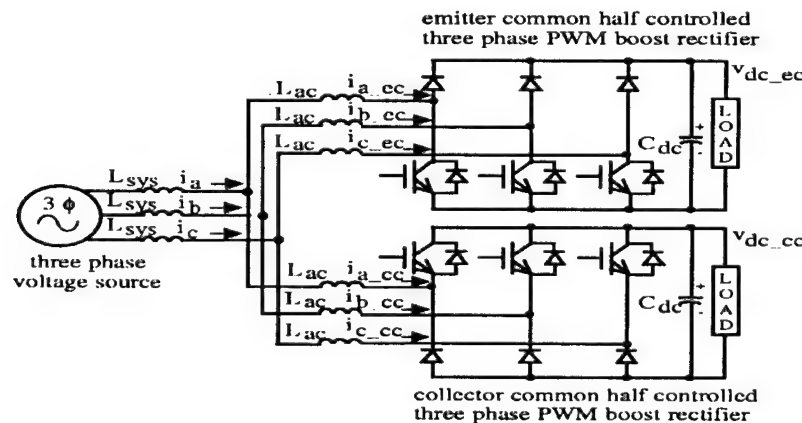


Figure 7-1 Complementary half controlled three phase PWM boost rectifier (rectifier leg complementary)

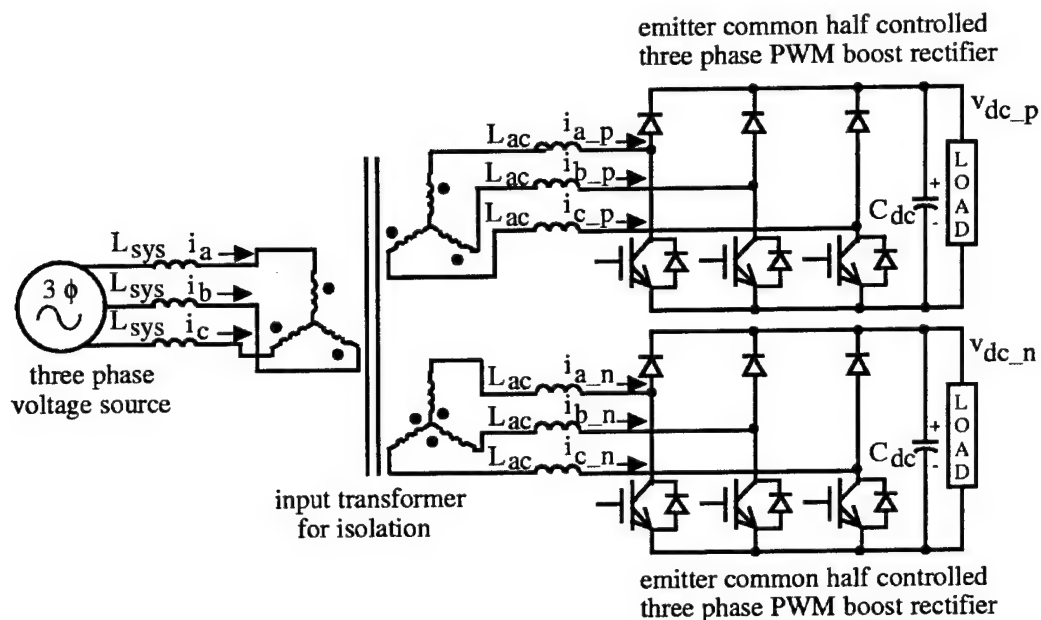


Figure 7-2 Complementary half controlled three phase PWM boost rectifier
(input transformer complementary)

7.3 Control schemes and simulation results

In this section, two control schemes for the complementary HC3ΦPWM boost rectifier and simulation results are presented. In the simulation, 600 [V] and 15 [A] (9 [kW]) of rated dc link voltage and current are assumed for each one of HC3ΦPWM boost rectifier with 230 [Vrms] line-to-line input voltage. In the simulation results to be presented, all the notations representing voltages and currents correspond to those in Figure 7-1 unless otherwise specified.

7.3.1 Independent local control (ILC)

If two loads supplied by a complementary rectifier are equal to each other, a simple independent local control (ILC) theoretically leads to even harmonic cancellation because their even harmonics are out of phase by 180 degrees. The advantage of this scheme is its straightforwardness since it simply involves replicating the control scheme proposed for the stand alone HC3ΦPWM boost rectifier [1].

Figure 7-3 shows *Saber* simulation results for a 25 [deg] lagging current command operation under a balanced load condition. The emitter common rectifier input currents,

i_{a_ec} , i_{b_ec} , and i_{c_ec} and the collector common rectifier input currents, i_{a_cc} , i_{b_cc} , and i_{c_cc} , are in the relation of inverted and 180 [deg] phase shifted with each other. Though each one of HC3 Φ PWM boost rectifier input current does not have half-wave symmetry, the overall input currents shown in Figure 7-3, i_a , i_b and i_c , regain half-wave symmetry and the even harmonics are eliminated. The non-triplen odd harmonics (5th, 7th, ...) are however still present as shown in this figure.

Figure 7-4 shows *Saber* simulation results for a 25 [deg] lagging current command operation with loads having 50 [%] imbalance. Since each half controlled rectifier is independently controlled, the load imbalance directly reflects on the overall input current even harmonic distortion.

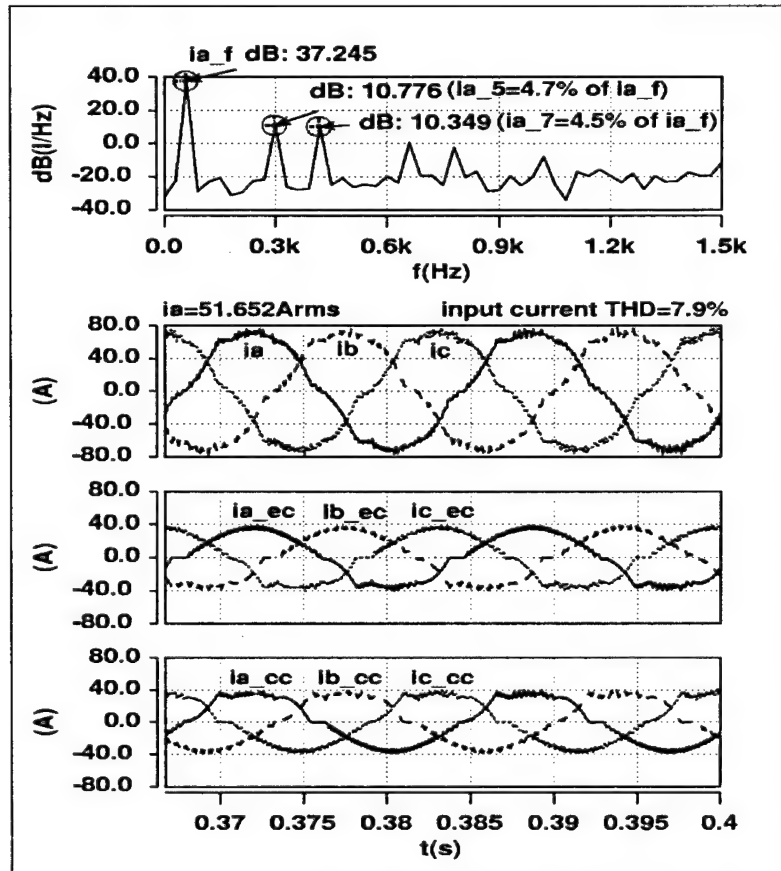


Figure 7-3 *SABER* simulation results of ILC for balanced load operation with 25 [deg] lagging current command (ac source 230 [Vrms] line-to-line, $L_{ac} = 3.1$ [mH] (0.2pu), dc link 600 [V] and 15 [A] for each dc link load, the top trace is spectrum of overall input current i_a)

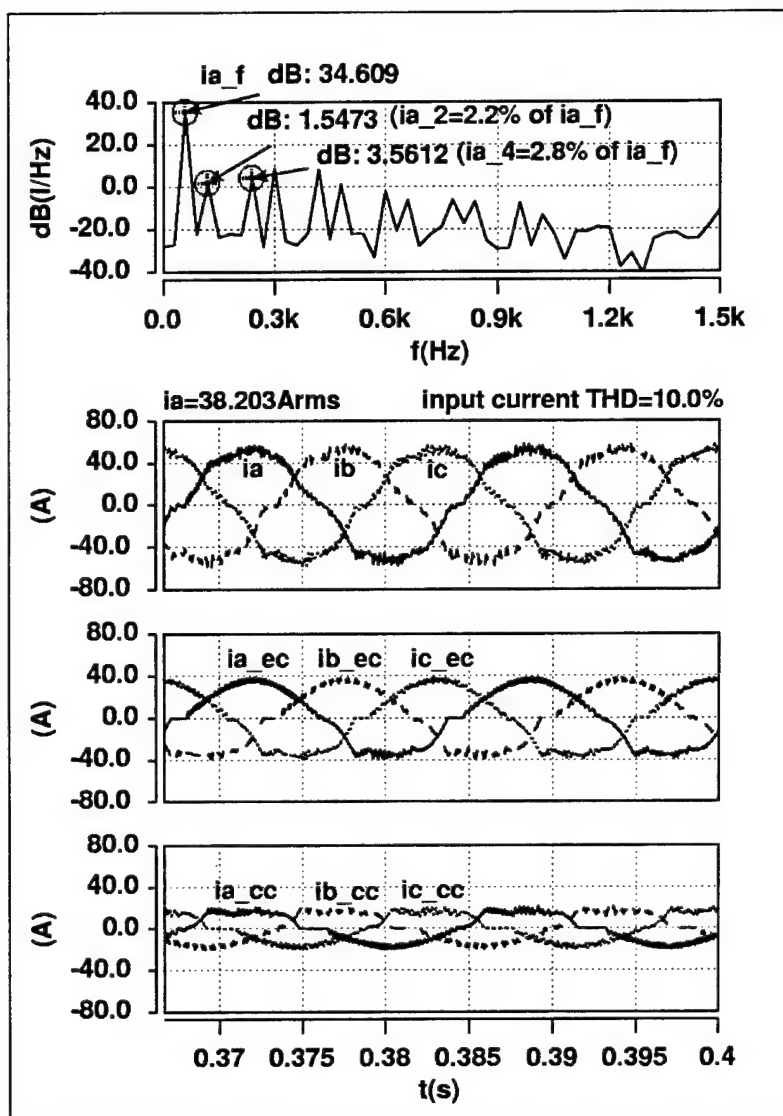


Figure 7-4 SABER simulation results of ILC for 50 [%] unbalanced load operation with 25 [deg] lagging current command (ac source 230 [Vrms] line-to-line, $L_{ac} = 3.1$ [mH] (0.2pu), dc link 600 [V] and dc load currents 15 [A] and 7.5 [A], the top trace is spectrum of overall input current i_a)

7.3.2 Coordinated central control (CCC)

A coordinated central control (CCC) is expected to be able to reduce the non-triplen odd harmonics in the overall input currents and to handle load imbalance to a certain extent.

Figure 7-5 shows a block diagram of CCC. Two proportional-integral (PI) control loops, one for each the sum and the difference of the two dc link voltages are used for the sinusoidal current reference amplitude calculation, where the PI controller gain of the dc

link voltage difference nulling is smaller than that of the dc link voltage sum regulating. The cross-coupled current feedback loops make it possible for each one of the HC3ΦPWM boost rectifiers to function as an active harmonic filter for the other. Here, the cut-off frequency of two low-pass filters (LPF's) on the cross coupling feedback paths is fairly important. If this cut-off frequency is too high, a current regulator unwantedly responds to the other one's switching frequency ripple. If it is too low, the desired mutual power filtering effect can not be obtained.

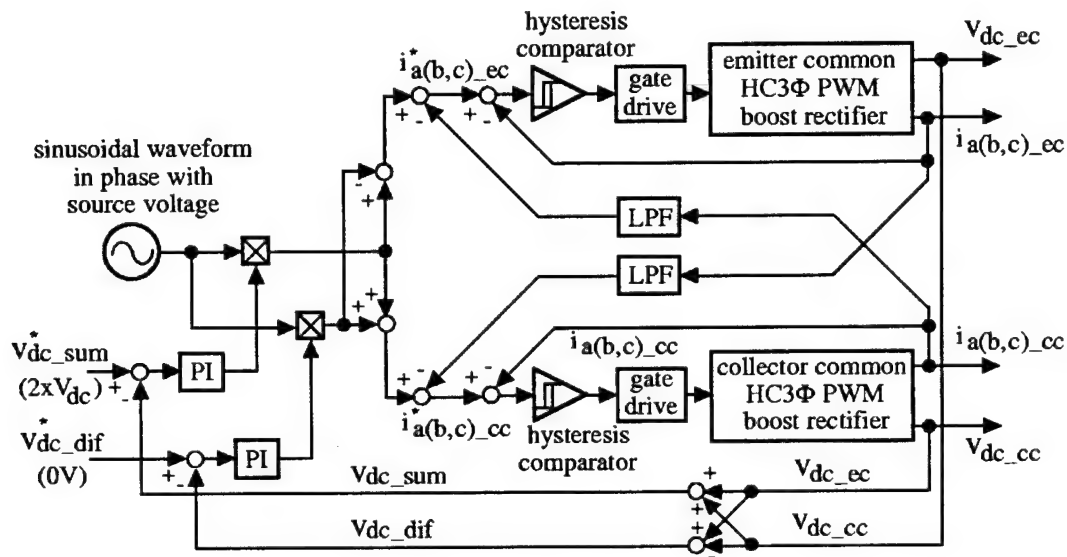


Figure 7-5 Block diagram of coordinated central control (CCC)

It is important to note here that each rectifier participates in controlling its own real power transfer and the other one's harmonic compensation simultaneously. This is a quite consistent approach with IEEE-519 which is not an equipment oriented harmonic standard but a point of common coupling (PCC) oriented standard [5], [6]. In addition, because of the mutual active filtering effect between the two HC3ΦPWM rectifiers, unlike ILC operation, not only the even harmonics but also non triplen odd harmonics are suppressed. This harmonic compensation performance now can make the ac side inductor size smaller than that of ILC operation, as far as the switching frequency limitation allows, and the lagging power factor current command operation is no longer necessary.

Figure 7-6 shows *Saber* simulation results for a balanced load operation. The ac side inductor size is 0.1 [pu] and the switching frequency of the hysteresis current controller is 7 ~ 13 [kHz] (beyond the range of the top trace in Figure 7-6). Without lagging power factor current command, much lower input current THD, 4.9 [%], is obtained.

Figure 7-7 shows *Saber* simulation results with loads having 50 [%] imbalance. Even with this amount of load imbalance, the even harmonics are still reasonably suppressed, and the input current THD is maintained at a fairly low level, 6.6 [%] in this simulation. These results suggest the potential of this approach for meeting IEEE-519 for systems whose short circuit ratio is as small as 20 [5].

Figure 7-8 and Figure 7-9 show *Saber* simulation results of dc link voltage ripples and dc load currents for a balanced and an unbalanced load condition, corresponding to Figure 7-6 and Figure 7-7, respectively. Each dc link capacitance is 1000 [μ F] and 0.1 [Ω] of equivalent series resistance (ESR) is assumed. The peak-to-peak dc link voltage ripple is approximately 3 [%] in both cases.

Almost the same simulation results have been obtained for *the input transformer complementary* HC3 Φ PWM boost rectifier, Figure 7-2.

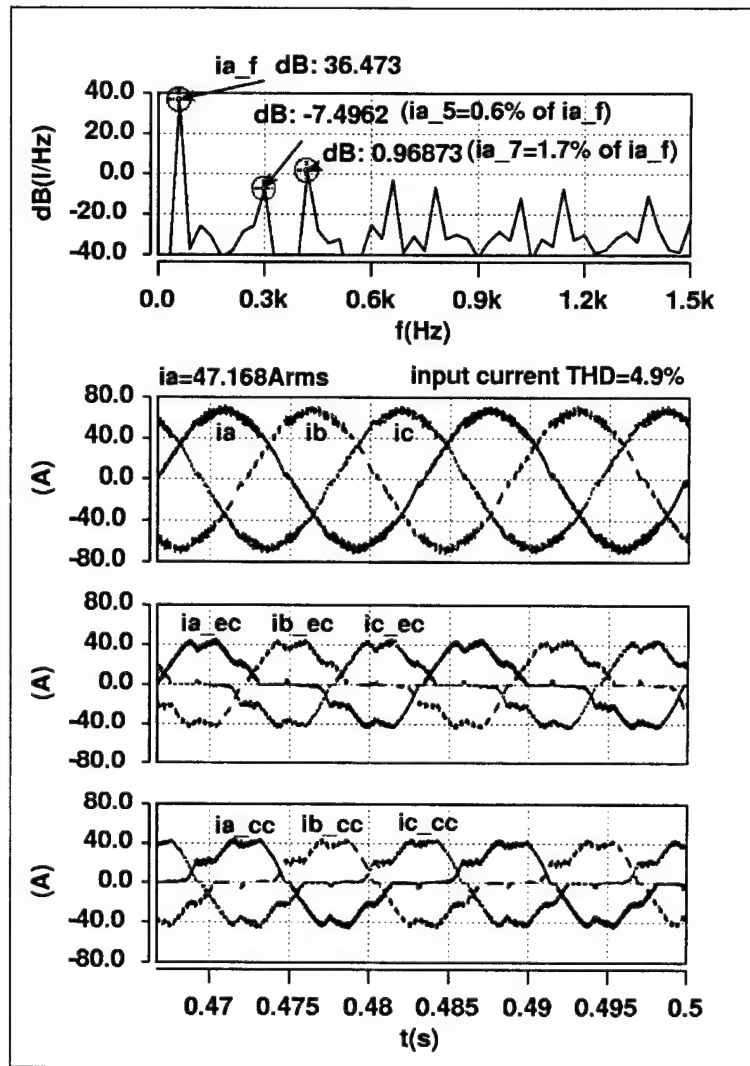


Figure 7-6 SABER simulation results of CCC for balanced load operation (ac source 230 [Vrms] line-to-line, $L_{ac} = 1.5$ [mH] (0.1pu), dc link 600 [V] and 15 [A] for each dc link load, the top trace is spectrum of overall input current i_a)

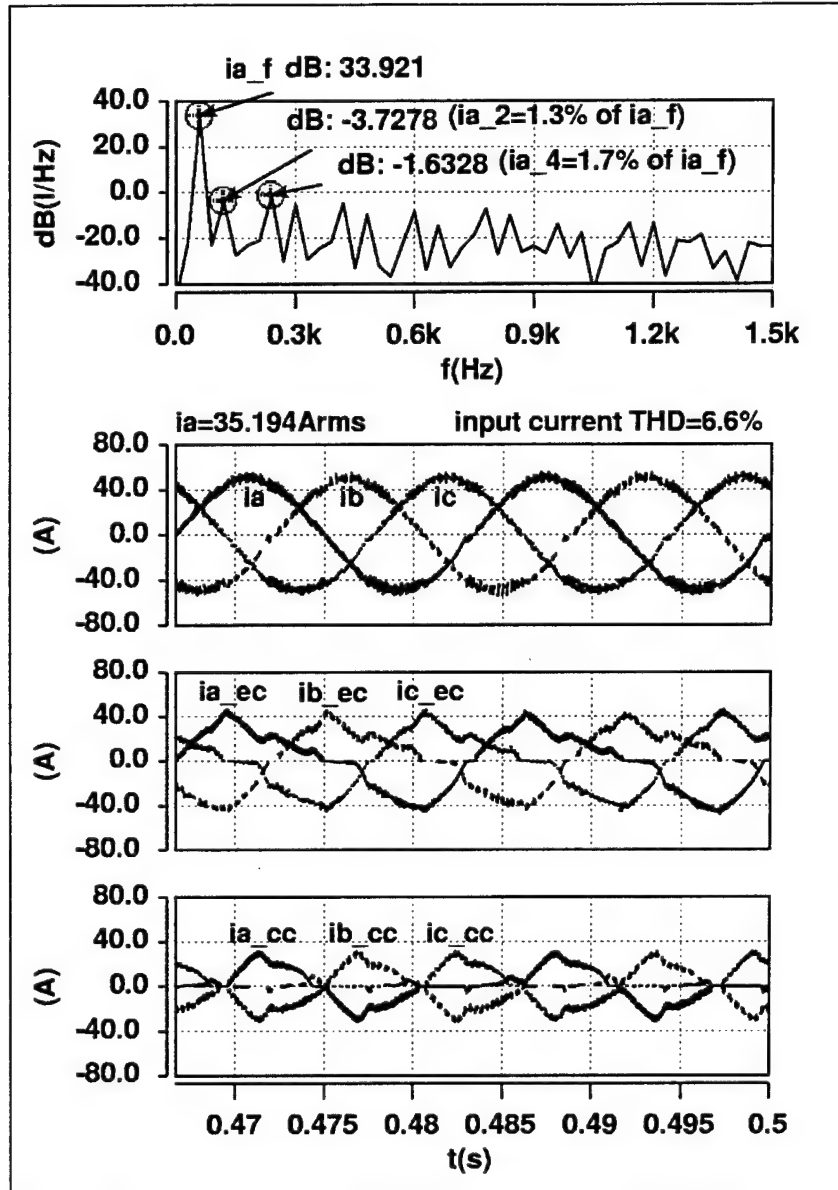


Figure 7-7 SABER simulation results of CCC for 50 [%] unbalanced load operation (ac source 230 [Vrms] line-to-line, $L_{ac} = 1.5$ [mH] (0.1pu), dc link 600 [V] and dc load currents 15 [A] and 7.5 [A], the top trace is spectrum of overall input current i_a)

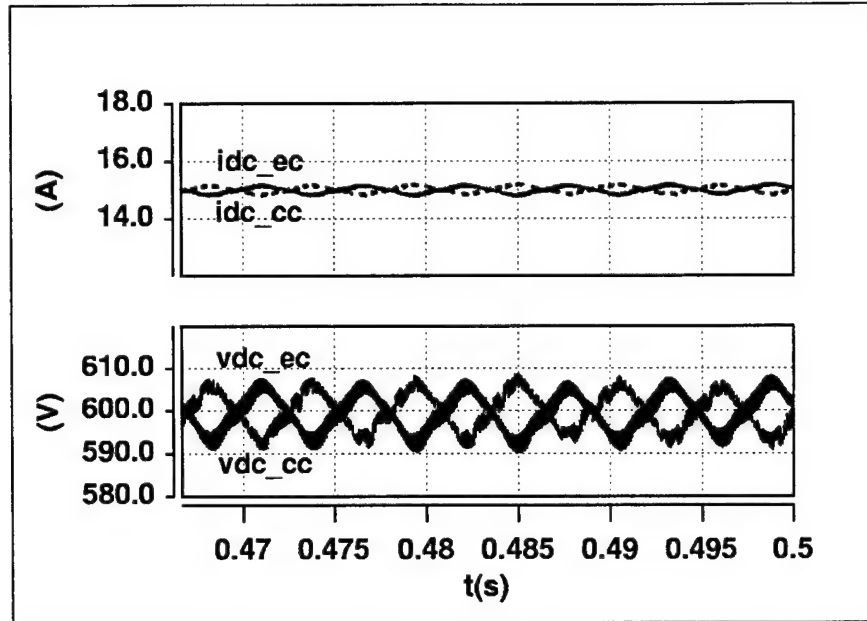


Figure 7-8 *SABER* simulation results of load current and dc link voltage ripple for balanced load operation with CCC ($C_{dc} = 1000$ [μ F] and $ESR = 0.1$ [Ω]). Operating condition is the same as that of Figure 7-6)

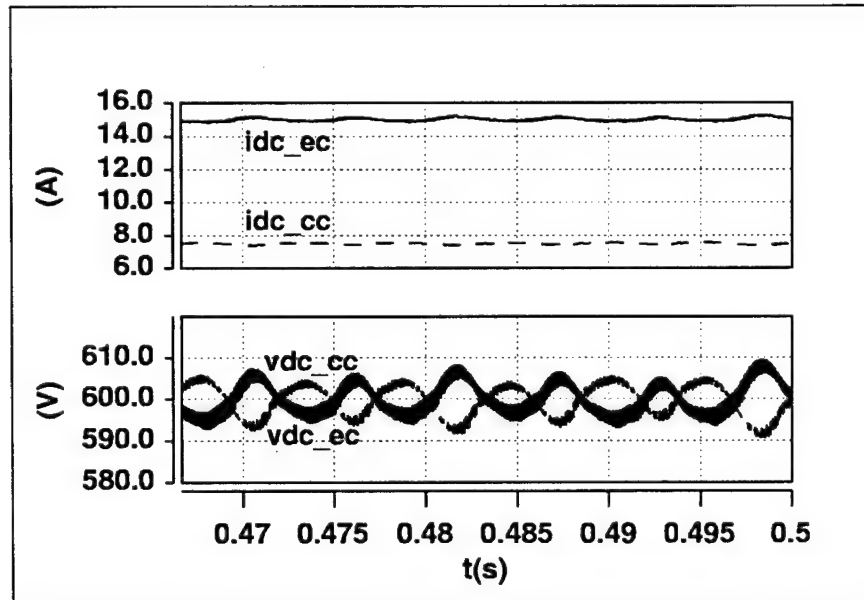


Figure 7-9 *SABER* simulation results of load current and dc link voltage ripple for unbalanced load operation with CCC ($C_{dc} = 1000$ [μ F] and $ESR = 0.1$ [Ω]). Operating condition is the same as that of Figure 7-7)

7.4 Experimental results

In this section, experimental results obtained with a laboratory prototype of the complementary HC3 Φ PWM boost rectifier are presented. This prototype is rated for 300 [V] and 7.5 [A] (2.25 [kW]) on each one of the dc links with 115 [V_{rms}] line-to-line voltage on the ac source side.

In the experiment, approximately 1.0 [%] of background distortion has been observed in the three phase ac source voltage.

A dynamic signal analyzer *HP 3561A* has been used for harmonic measurement. The spectra presented here are rms averaged results of 256 measurements.

7.4.1 Independent local control (ILC)

Figure 7-10 and Figure 7-11 show experimental ac current waveforms and overall input current spectrum, respectively, for ILC with balanced loads, where line-to-line voltage v_{cb} , trace1, is shown along with the input current for phase reference purpose. The maximum point of v_{cb} which coincides with the origin point of time axis is 0 [deg] reference for unity power factor angle. The current waveforms are in reasonably good agreement with the corresponding simulation results shown in Figure 7-3. The measured input current THD is 7.0 [%]. This value is slightly better than that of the simulation result. The probable cause of this is that the equipment used for harmonic measurement is capable of THD computation with first 20 harmonics [7]. This is the case for all the following experimentally measured THD values.

Figure 7-12 and Figure 7-13 show experimental results for ILC with loads having an imbalance of about 50 [%], which correspond to Figure 7-4.

In Figure 7-10 through Figure 7-13, compared to stand alone operation results presented in reference [1], the even harmonics are well suppressed, although the perfect even harmonic cancellation can not be realized even with balanced loads. This is because that it is difficult to achieve the exact complementary operation in practical situations. In

Figure 7-13, it is observed that the second harmonic is decreased with the load imbalance. The cause of this rather strange phenomenon is currently under investigation. As expected, the non triplen odd harmonics observed here are fairly large.

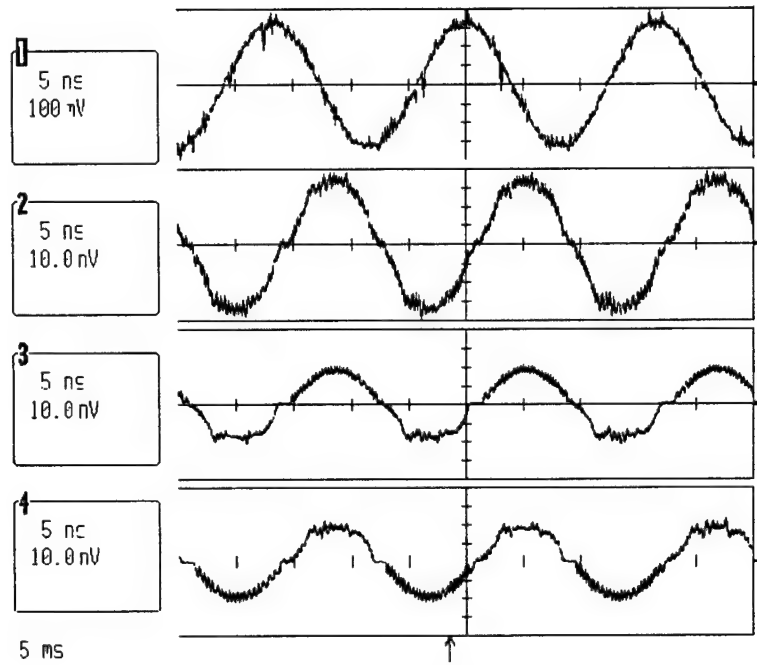


Figure 7-10 Experimental results of ILC for balanced load operation with 25 [deg] lagging current command (ac source 117 [Vrms] line-to-line, $L_{ac} = 3.1$ [mH] (0.2pu), dc link 300 [V] and 7.5 [A] for each dc link load), trace 1: v_{cb} , 50 [V/div], trace 2: i_a , trace 3: i_{a_ec} , trace 4: i_{a_cc} , 10 [A/div], time axis 5 [ms/div]

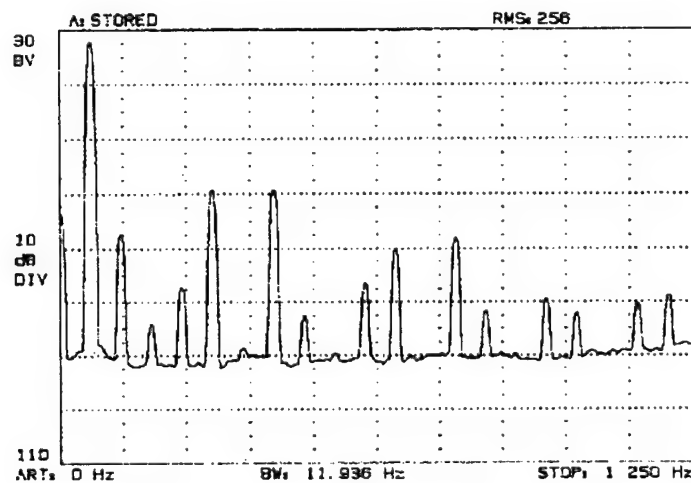


Figure 7-11 Experimental spectrum of overall input current i_a in Figure 7-10, THD = 7.0 [%] (computed with up to the 20th harmonic)

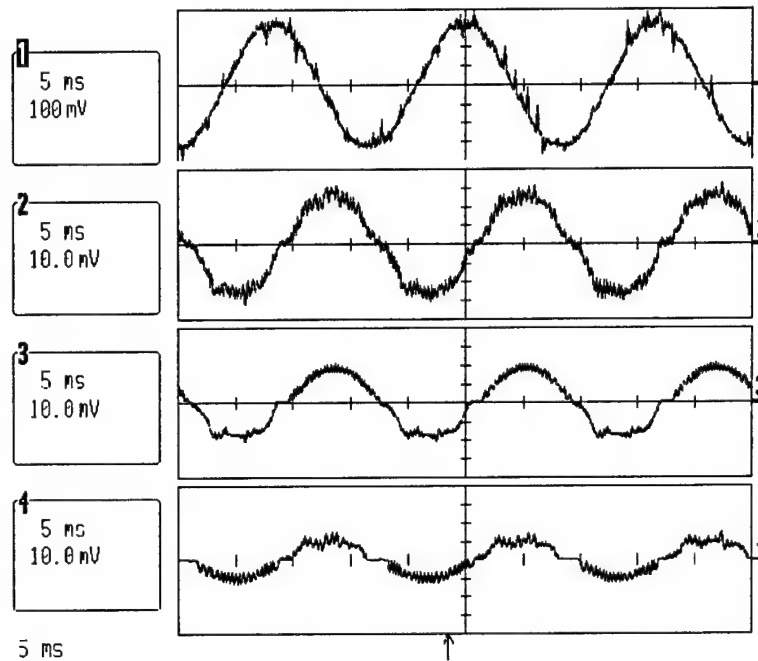


Figure 7-12 Experimental results of ILC for unbalanced load operation with 25 [deg] lagging current command (ac source 117 [Vrms] line-to-line, $L_{ac} = 3.1$ [mH] (0.2pu), dc link 300 [V] and dc load current 7.5 [A] and 4.4 [A]), trace 1: v_{cb} , 50 [V/div], trace 2: i_a , trace 3: i_{a_ec} , trace 4: i_{a_cc} , 10 [A/div], time axis 5 [ms/div]

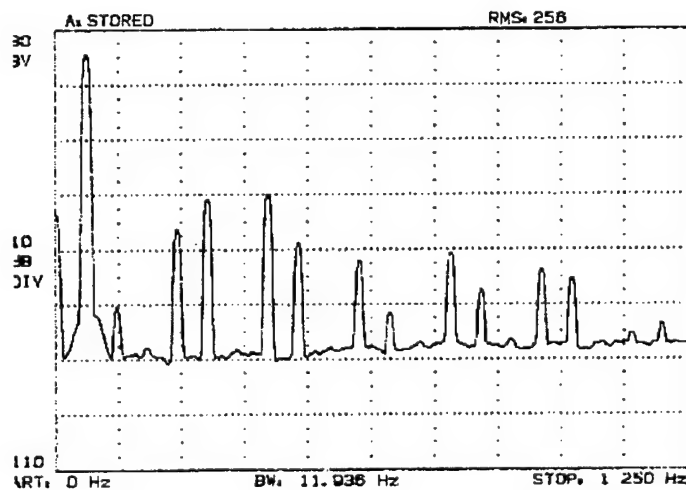


Figure 7-13 Experimental spectrum of overall input current i_a in Figure 7-12, THD = 8.3 [%] (computed with up to the 20th harmonic)

7.4.2 Coordinated central control (CCC)

In the hardware experiments for CCC, unity power factor current command is maintained and the ac side inductor value has been reduced from 0.2 [pu] of ILC to 0.1 [pu].

Figure 7-14 and Figure 7-15 show experimental ac current waveforms and overall input current spectrum, respectively, for CCC with balanced loads. These are in reasonably good agreement with corresponding simulation results shown in Figure 7-6.

Compared to experimental results of ILC shown in Figure 7-10, the overall input current waveform is closer to sinusoid. This is because, as observed in the spectrum of Figure 7-15, not only even harmonics but also non-triplen odd harmonics are reduced by CCC. In addition, phase relation between v_{cb} and i_a shows that almost unity power factor operation is realized.

Figure 7-16 and Figure 7-17 show experimental results for CCC with loads having an imbalance of about 50 [%]. It may be observed that current waveforms are in reasonably good agreement with those of simulation results shown in Figure 7-7. With this load imbalance, the overall input current, i_a , is still maintained to be fairly sinusoidal.

Figure 7-18 and Figure 7-19 show experimental dc link voltage ripple for a balanced and an unbalanced load condition, corresponding to Figure 7-14 and Figure 7-16, respectively. Similar to the simulation results of Figure 7-8 and Figure 7-9, 180 [Hz] ripple is dominant and its peak-to-peak magnitude is approximately 4 [%] of the dc link voltage.

Figure 7-20 shows measured characteristics of load imbalance vs. low order harmonics with respect to fundamental component, I_f , and THD, where the load imbalance is expressed as the ratio of R_{dc_cc} to R_{dc_ec} with $R_{dc_ec} = 1.0$ [pu]. Then, the operating condition of Figure 7-12 and Figure 7-16, i.e. $i_{dc_ec} = 7.5$ [A] and $i_{dc_cc} = 4.4$ [A], corresponds to $R_{dc_cc}/R_{dc_ec} = 1.7$. According to this measured data, 4th and 7th harmonics are fairly well suppressed, and 2nd and 5th harmonics increase as the dc link load imbalance increases, and accordingly THD increases.

Referring to IEEE-519, even harmonics are limited to 25 [%] of the odd harmonic limits [5]. For example in the case of a system with short circuit ratio, $20 < I_{sc}/I_L < 50$, 2nd harmonic component should be less than 1.75 [%] of I_L . Since I_L is the maximum demand load current fundamental component at PCC and $I_f \leq I_L$, the measure taken in Figure 7-20 is a more conservative metric, similar to the difference between THD and the total demand distortion (TDD).

The judgment on if or not a system can satisfy a harmonic standard such as IEEE-519 should be based on measurement with long term operation. In addition, even harmonic limitation monitoring involves fairly subtle measurement because of its even less maximum limit. However, it has been demonstrated here on a laboratory experiment basis that the complementary HC3 Φ PWM rectifier with CCC has a potential to realize a rectifier front-end for multi-dc-link applications with meeting IEEE-519 standard.

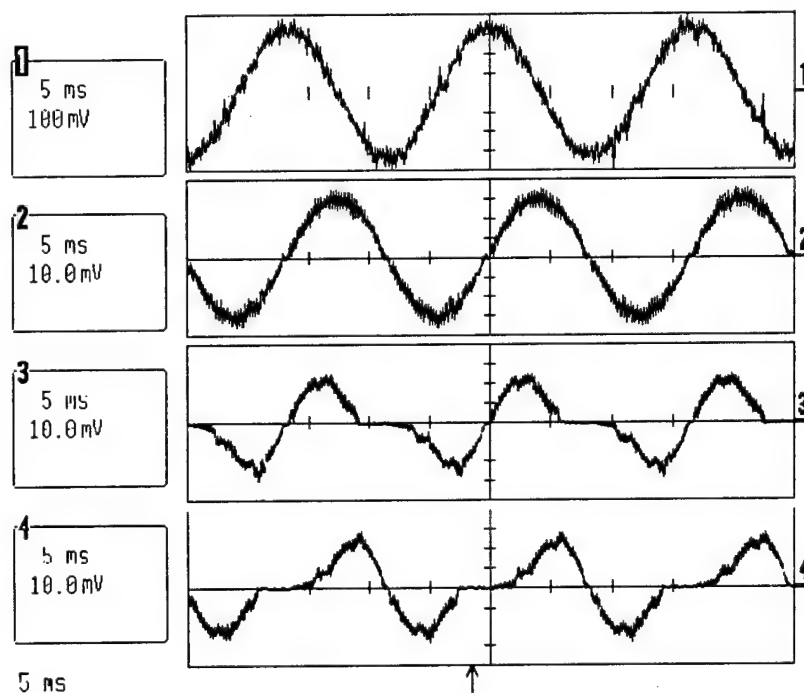


Figure 7-14 Experimental results of CCC for balanced load operation with unity power factor current command (ac source 117 [Vrms] line-to-line, $L_{ac} = 1.5$ [mH] (0.1pu), dc link 300 [V] and 7.5 [A] for each dc link load), trace 1: v_{cb} , 50 [V/div], trace 2: i_a , trace 3: $i_{a_{ec}}$, trace 4: $i_{a_{cc}}$, 10 [A/div], time axis 5 [ms/div]

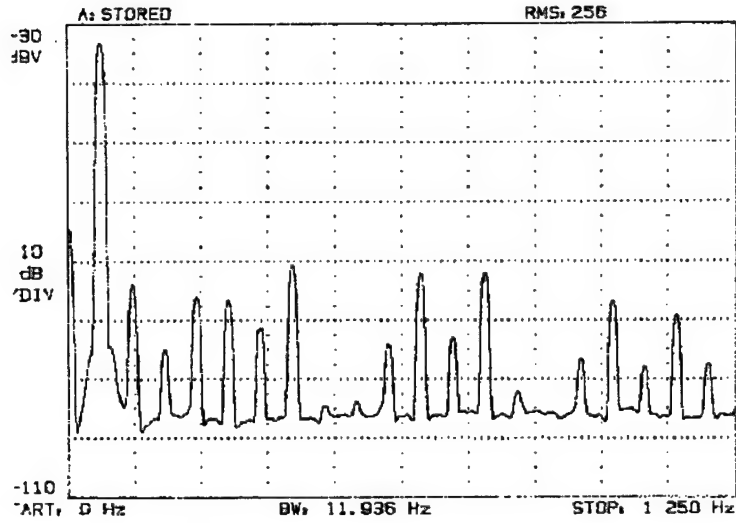


Figure 7-15 Experimental spectrum of overall input current i_a in Figure 7-14, THD = 2.8 [%]
(computed with up to the 20th harmonic)

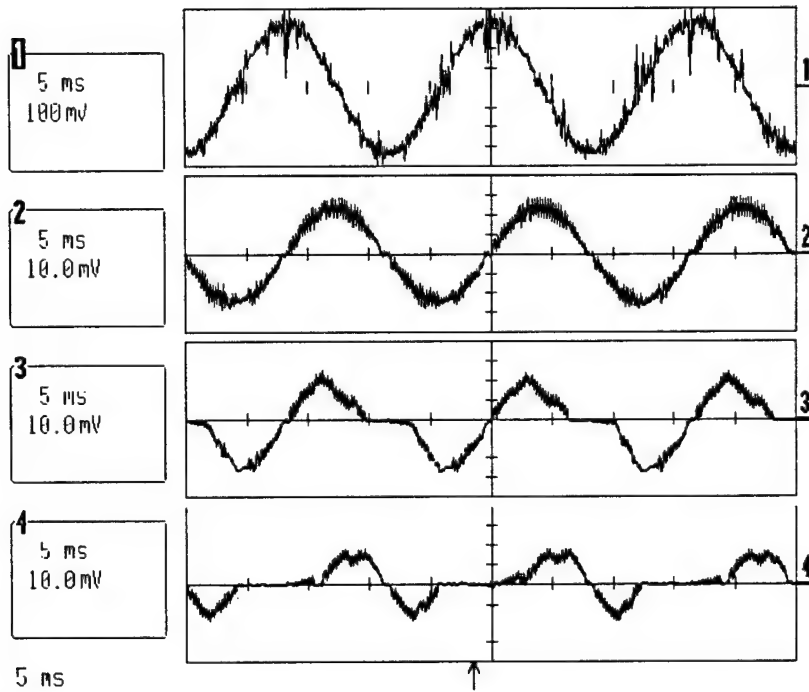


Figure 7-16 Experimental results of CCC for unbalanced load operation with unity power factor current command (ac source 117 [Vrms] line-to-line, $L_{ac} = 1.5$ [mH] (0.1pu), dc link 300 [V] and dc load current 7.5 [A] and 4.3 [A]), trace 1: v_{cb} , 50 [V/div], trace 2: i_a , trace 3: i_{a_ec} , trace 4: i_{a_cc} , 10 [A/div], time axis 5 [ms/div]

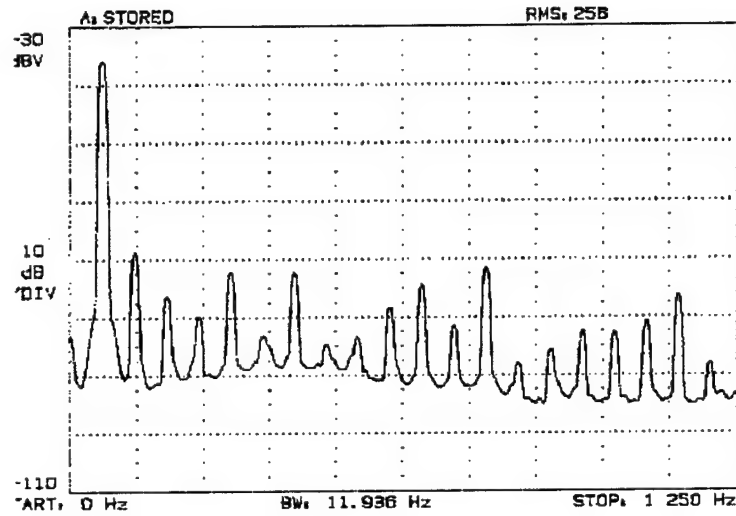


Figure 7-17 Experimental spectrum of overall input current i_a in Figure 7-16, THD = 4.2 [%]
(computed with up to the 20th harmonic)

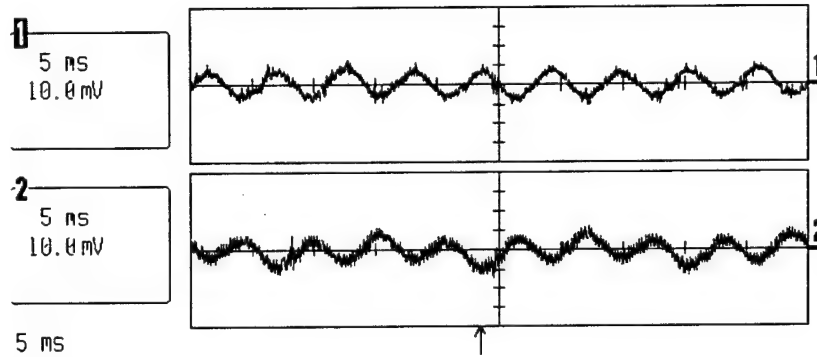


Figure 7-18 Experimental dc link voltage ripple of CCC for balanced load operation of Figure 7-14
($C_{dc} = 1250$ [μ F]), trace 1: $v_{dc_{ec}}$, trace 2: $v_{dc_{cc}}$, 5 [V/div], time axis 5 [ms/div]

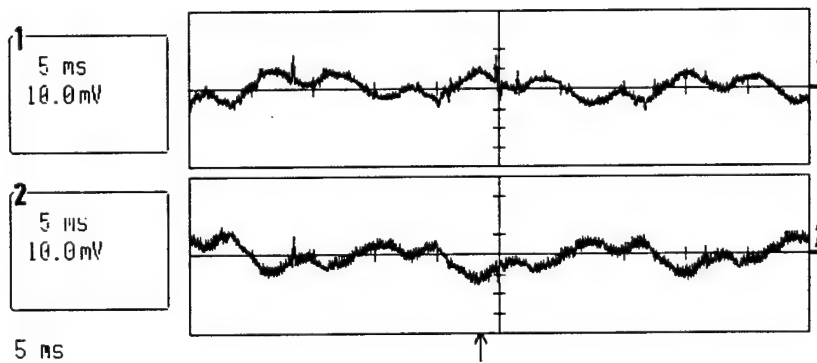


Figure 7-19 Experimental dc link voltage ripple of CCC for unbalanced load operation of Figure 7-16
($C_{dc} = 1250$ [μ F]), trace 1: $v_{dc_{ec}}$, trace 2: $v_{dc_{cc}}$, 5 [V/div], time axis 5 [ms/div]

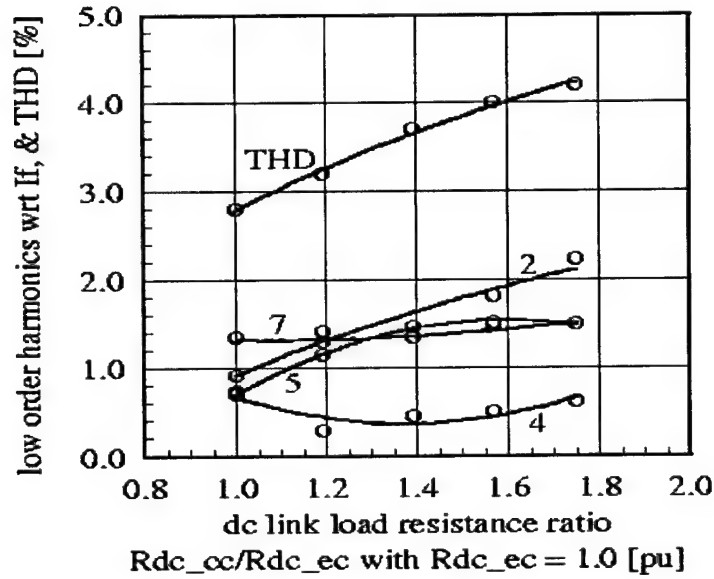


Figure 7-20 Experimentally measured characteristics of load imbalance vs. low order harmonics with respect to fundamental component I_f and THD for CCC (THD is computed with up to the 20th harmonic)

7.5 Conclusions

The complementary HC3ΦPWM boost rectifier for multi-dc-link applications has been investigated. It has been shown that the main disadvantages associated with stand alone operation of HC3ΦPWM boost rectifier, i.e. even harmonic input current distortion, large ac side inductor, and lagging power factor current command operation for low THD, can greatly be mitigated by the approach presented here.

Two control schemes, ILC and CCC, have been introduced and their performance has been studied with simulations and hardware experiments. In particular, it has been demonstrated that CCC has a capability to reduce not only even harmonics but also non-triplen odd harmonics and has potential to meet IEEE-519 with certain dc link load imbalance handling capability.

In this paper, *the rectifier leg complementary* structure, Figure 7-1, has almost exclusively been discussed. However, as mentioned in Section III, the same simulation results have been obtained for *the input transformer complementary* structure, Figure 7-2. Experimental work on *the input transformer complementary* configuration is currently under progress.

So far, only the steady state operation characteristics of the complementary HC3 Φ PWM boost rectifier have been studied mainly from the power quality point of view. Since, unlike diode rectifiers, HC3 Φ PWM boost rectifiers are capable of active dc link voltage control, the dynamic characteristics is another issue of interest. For example, if the system could handle the voltage sag problem to a certain extent, or could manage to softly recover from an ac source voltage upset, this would be an added advantage of HC3 Φ PWM boost rectifier front-end. The dynamic characteristic investigation should be one of the focuses for future work.

7.6 References

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Chapter 8 Stand-Alone High Power Tests and Associated Issues in the 100kW Soft-Switched DC Bus Regulator

8.1 Introduction

In the last phase of the research on the 100kW soft-switched DC bus regulator, the converter system was built and the functional tests were completed. In order to fulfill the tasks of this bus regulator in the proposed DC distributed power system, the power level has to be pushed to very high, and the DC bus voltage should reach 800V. Therefore, the main task in this phase of the research work is to complete the high power tests of the bus regulator and solve the associated issues that may occur in both hardware and software under high power levels. Another task in this phase of the work is to reconfigure this PEBB converter as a motor drive inverter to demonstrate the concept of the PEBB modules and their plug and play (PNP) at the PCIM'99 show in Chicago. Control software for a butterfly valve has been developed for this purpose.

This DC bus regulator has six main IGBT switches for power factor correction (PFC) as well as DC output regulation, and another six auxiliary IGBT switches for zero current transition (ZCT) soft switching. With the additional passive components, sensors, a DSP-EPLD controller and various auxiliary power supplies for the converter, it is not a simple system for either the power stage or the controller. For this reason, it is necessary to do the high-power tests step by step. All the bugs have to be found and eliminated before they damage to the system.

Fortunately, by adopting the PEBB concept, the power stage of this DC bus regulator is made of three of the same ZCT PEBB modules. Therefore, each PEBB module can be tested separately. After this, the PEBB modules can be put together, and the system can be operated as an open-loop three-phase inverter. The space vector modulation (SVM) algorithm, which is the core part of the digital controller, can be verified using the inverter mode. The ZCT soft-switching technique in three-phase PWM converter applications also can be tested by the inverter mode. The third test is the PFC rectifier mode test. Since the PWM rectifier mode requires closing both the current and voltage

loops, the parameters of the digital controller have to be designed carefully. All the sensors have to be calibrated accurately beforehand. This report will give a detailed description of the entire test processes and issues. Important test results of this 100 kW soft-switched DC bus regulator will also be presented.

8.2 Test on ZCT Soft-Switching PEBB Modules

8.2.1 Test circuit setup

The first stage of the converter test is the high-power tests on individual PEBB modules. As was described in last year's project report, the ZCT soft-switching PEBB module can be regarded as a combination of two soft-switching cells, as shown in Figure 8-1. The shaded area is one of the two soft-switching cells. Due to the symmetry of the two soft-switching cells, the PEBB module test can be further divided into the soft-switching cell test.

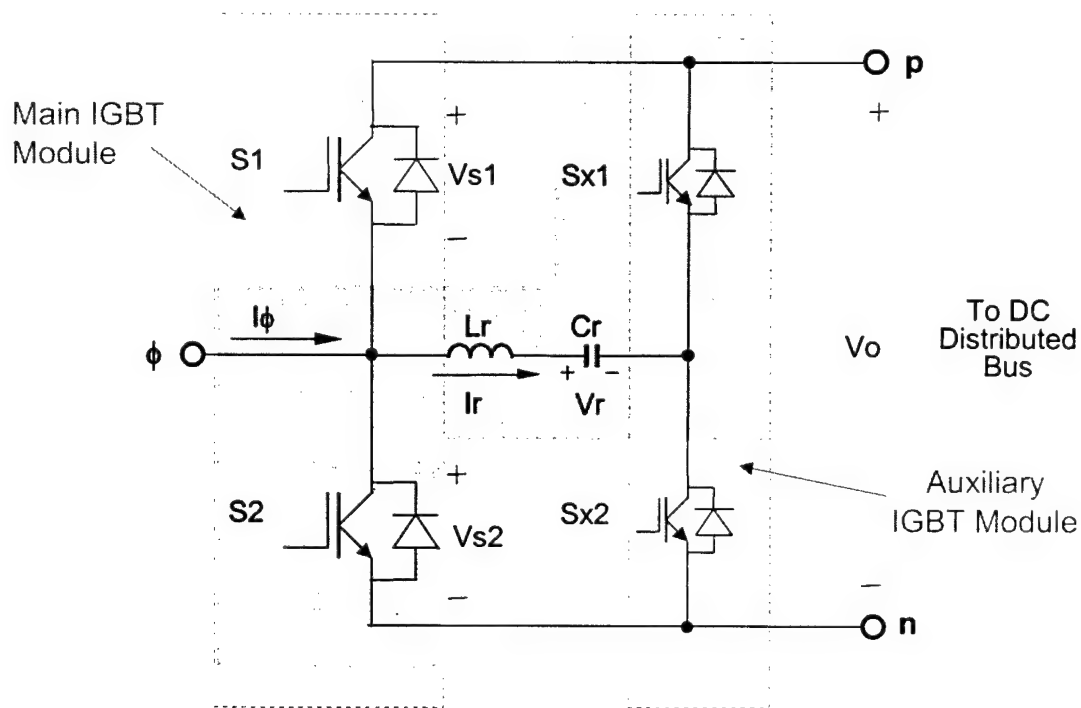


Figure 8-1. Topology of a ZCT PEBB Module.

Each soft-switching cell can be configured as a boost, buck or other type of DC-DC converter topology. The objective is to test each soft-switching cell up to its maximum

power level when it is working in a three-phase converter under the same voltage stress. Since the available resistance of the load bank is very low for high-power tests, each soft-switching cell is configured as a buck converter in the tests. The configuration of the test setup for the lower soft-switching cell is shown in Figure 8-2.

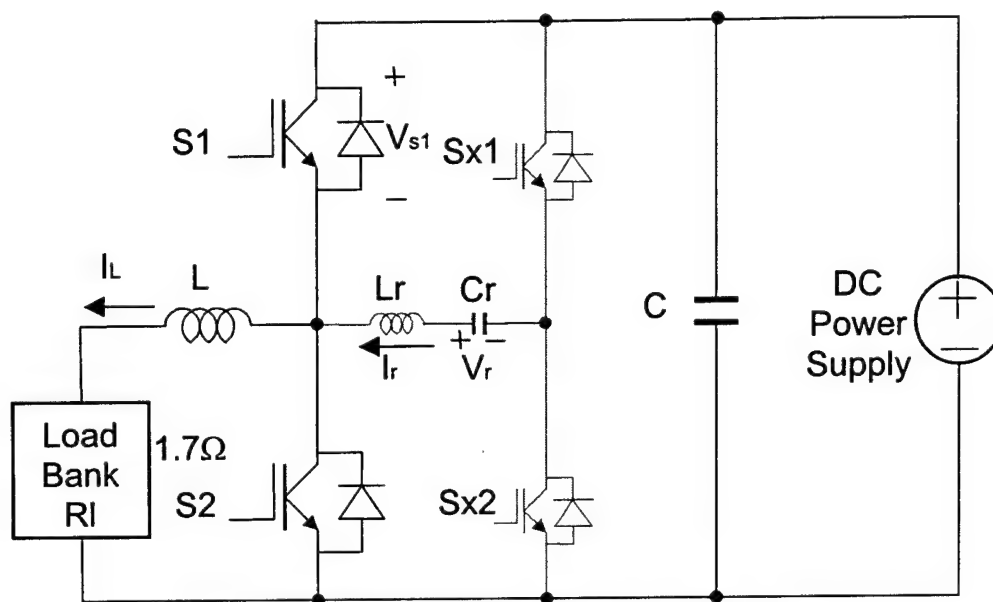


Figure 8-2. Test setup for a single ZCT PEBB module.

8.2.2 Determine switching frequency

Switching frequency should be decided before the tests. To push the switching frequency to get high performance for the converter is one of the major objectives of designing the ZCT PEBB modules. However, the switching frequency is limited by switching loss and also by soft-switching techniques due to the associated duty cycle loss. The power capability of the IGBT gate drive circuit is also a concern. Switching frequency tests on the adopted IGBT gate drive circuit were conducted. As shown in Figure 8-3, several different gate resistances (from 2.2Ω to 11Ω) were used to investigate the input power dissipation versus the switching frequency. As shown in Figure 8-3, the gate resistance does not affect the frequency characteristic of the gate drive power dissipation. The rated output power of the two DC-DC power supplies on the IGBT gate drive board is 1W each. Considering the different power consumptions in the positive and negative power supplies, the total power capability of the two power supplies is estimated as 1.5W. Therefore, a reasonable switching frequency limit for the adopted gate drive is 35kHz

from the curve plots. Since the minimal pulse width for the soft-switching operation is about $6\mu\text{s}$, 20kHz-switching frequency is chosen to minimize the negative effect of the pulse width limit on PWM operation. This issue will be illustrated later in this chapter.

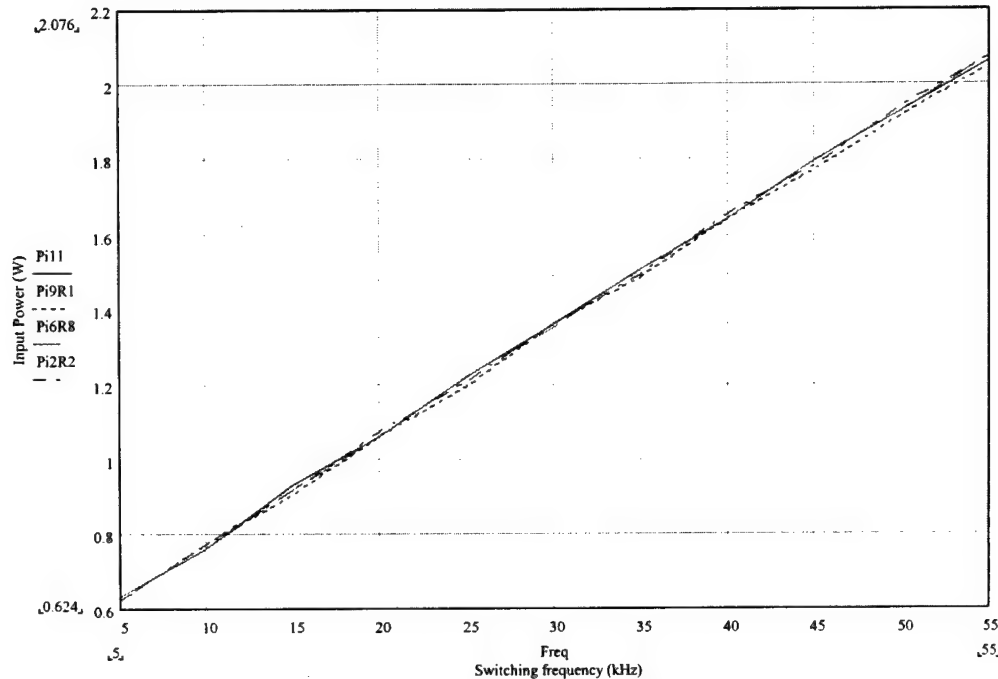


Figure 8-3. Plots of the input power of gate drive board vs. switching frequency with different turn-on resistor.

8.2.3 Test on protection threshold

The protection mechanism of the IGBT gate drives was also tested. The protection threshold for the main IGBT switches was set to 450A to enable the soft-switching operation. The burst mode of the signal generator (HPE3631A) was used to achieve the single pulse trigger. In the burst mode, the pulse width of the trigger signal can be adjusted to charge the inductor current to exceed the protection threshold. DC bus voltage determines the slope of the inductor current. The test waveforms are shown in Figure 8-4.

In Figure 8-4, channel 2 is the current waveform of the IGBT switch (100A/div). Channel 3 is the IGBT switch voltage waveform. The inductor turns out to saturate at about 360A. After the saturation, the switch current increases sharply. This happens to be the case when short-circuit occurs in the switch. The actual threshold is about 456A.

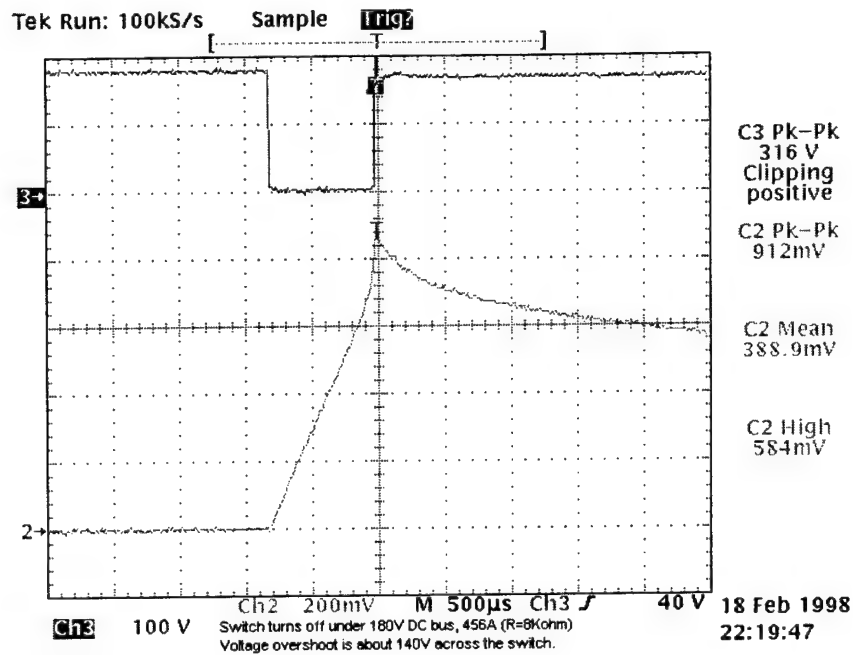


Figure 8-4. Protection test waveforms.

8.2.4 Test results for ZCT soft-switching PEBB modules

The operating switching frequency is 20kHz with the soft-switching function enabled. The input voltage is cranked up to 800V, and the output power is adjusted to 18.3kW to emulate the voltage and the processing power of every soft-switching cell in a 100kW PFC rectifier operation. The test waveforms are shown in Figure 8-5.

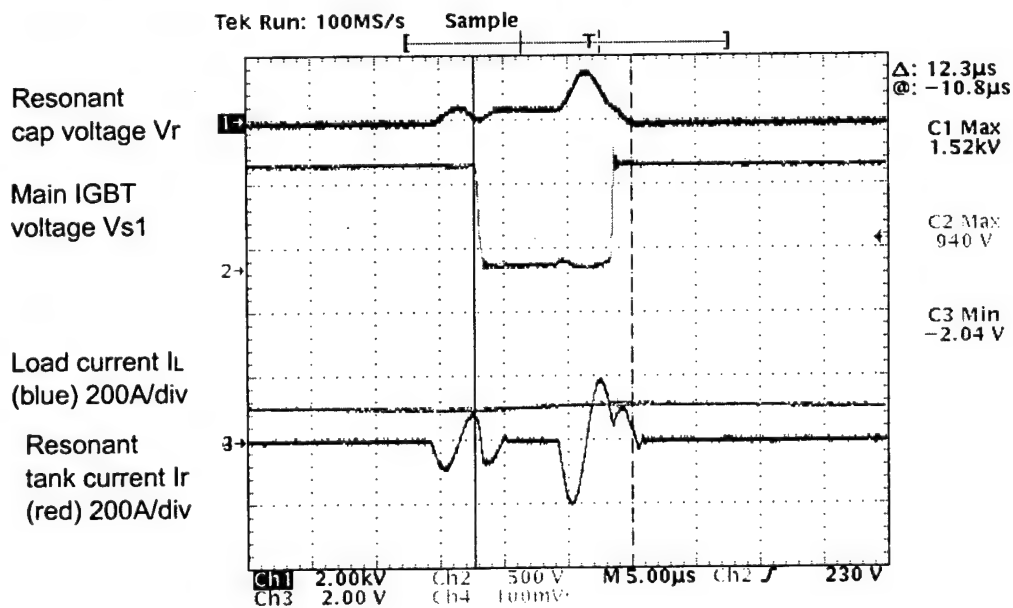


Figure 8-5. ZCT PEBB module with 20kHz switching frequency.

All the PEBB modules are tested up to their rated operating power level. It takes quite a while to complete all the tests. However, the high-power tests prove the solid performance of the PEBB modules of this converter.

8.3 Electrical and thermal issues on power stage components

Due to the high power level of the PEBB modules, both the active and passive components of the power stage have high electrical and thermal stress. For the PEBB modules, the ZCT soft switching reduces the switching loss significantly, but the high conduction loss and high switching frequency still cause thermal issues.

A group of test data on PEBB modules is presented to show the thermal issues in the power stage. Figure 8-6 shows temperature rise of the case for the main IGBT switch. The room temperature is 24°C, and the heat sink is cooled by 21°C flowing water. All the test data are recorded after 30 minutes of operation. In Figure 8-6, the IGBT case temperature reaches 64°C when the input power is equal to 18kW. This temperature is too much for the IGBT switch, and failure occurs at this point.

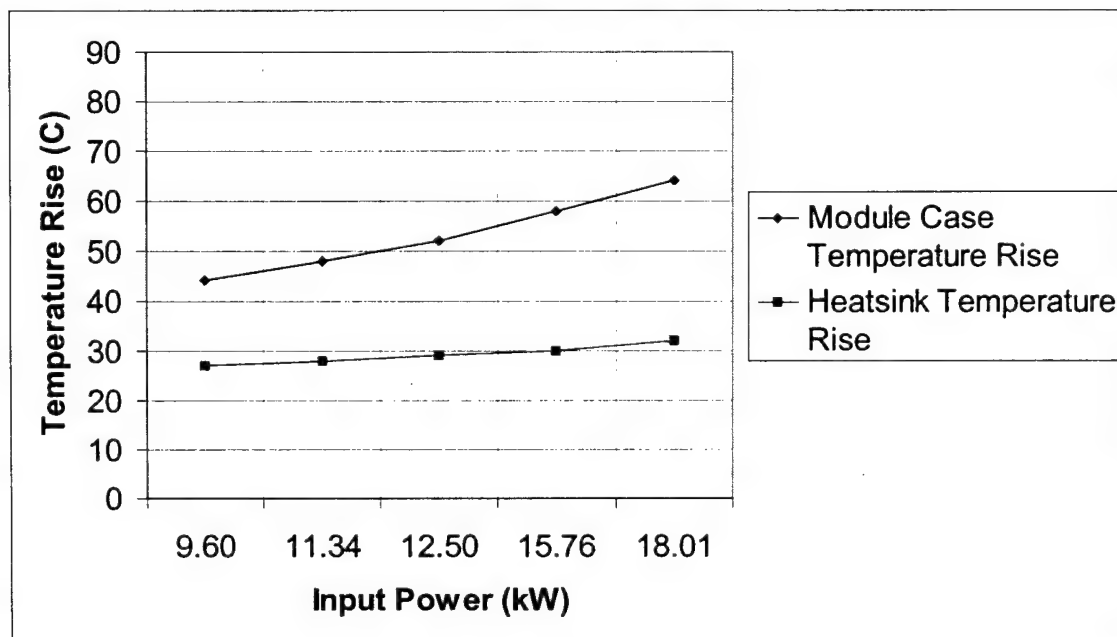


Figure 8-6. Temperature rise for module case and heat sink.

Since the 18kW input power for one switch is similar to the 100kW for six switches, the thermal issue will not allow this converter to run at the 100kW power level. Actually, the situation at 100kW is worse; there are two reasons for this issue. One is that the power dissipation capability of the heat sink under the same cooling condition is fixed. But the power loss for six switches is six times that of one switch, if we assume one switch in three-phase operation has the same loss as in DC-DC operation when handling the same power. The reason is that the power loss doubles in one package. The doubled power loss will result in higher case temperature rise. Therefore, lower temperature cooling water should be used, and the flow speed should be increased to achieve better thermal management.

For the soft-switching circuit, the high-voltage, high-current resonance with very high frequency occurs at the turn on and off transition in the resonant tank. The electrical and thermal stress becomes a concern. The plot of the temperature rising in resonant capacitor versus DC bus voltage is shown in Figure 8-7. The steady-state temperature of the resonant capacitor exceeds its rating (80 C) before the DC bus reaches 800V. The 800V DC bus test was done in a relatively short time before the temperature of the resonant tank went too high.

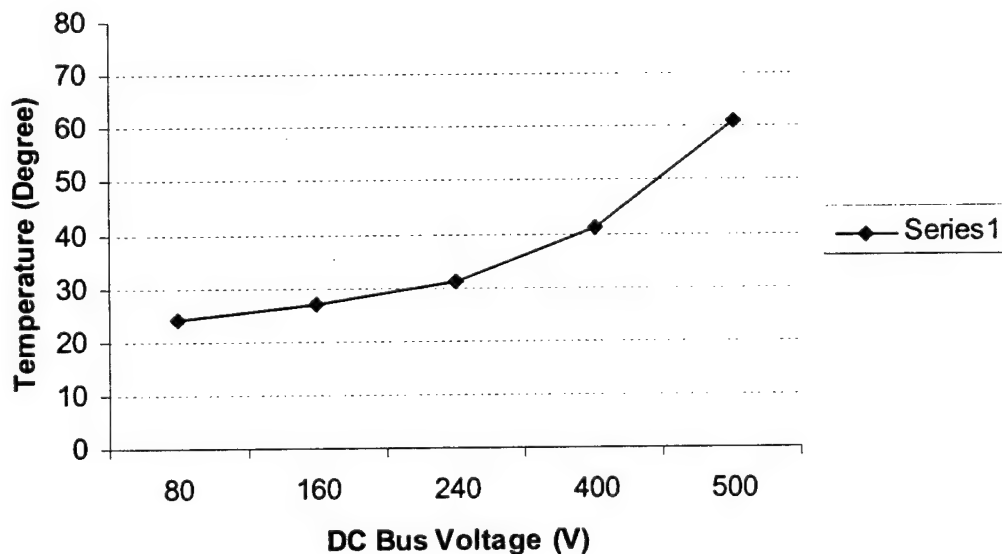


Figure 8-7. Temperature measurement for the resonant capacitor.

It is evident that the existing heat dissipation capability in the test setup is not sufficient to deal with the thermal stress in the resonant tank. The RMS current of the resonant tank almost reaches the rated value of the resonant capacitor (50A RMS) from the measurement under 800V. Resonant capacitors with higher current and better thermal capability may have to be chosen for this reason. However, it is difficult to find a resonant capacitor that can withstand high peak voltage, high RMS current and low profile that can accommodate the current PEBB module. This problem is finally resolved by the SVM scheme adopted in controlling this three-phase converter.

8.4 Inverter Mode Test with Soft Switching

8.4.1 Significance of the inverter mode test with ZCT soft switching

The inverter mode test is very important for this DC bus regulator. The topology is identical for both the inverter and rectifier modes. The main difference is that the direction of their power flow is reversed. This makes the inverter mode like a buck converter, and the rectifier mode like a boost converter. Therefore, completing the high power tests in inverter mode can make sure the ZCT PEBB modules will work well in three-phase PWM operation.

From the control aspect, the boost rectifier mode has to use closed-loop control to achieve the unity power factor and tightly regulated output DC voltage, while the open-loop control is enough for the inverter mode. The modulation strategies and the digital controller are almost the same in the two different operation modes. We can regard the inverter mode as somewhat similar to the open-loop mode of the PFC rectifier. Therefore, the inverter mode greatly facilitates the debugging of the controller and modulation techniques for the DC bus regulator. The circuit diagram for the inverter mode test is shown in Figure 8-8.

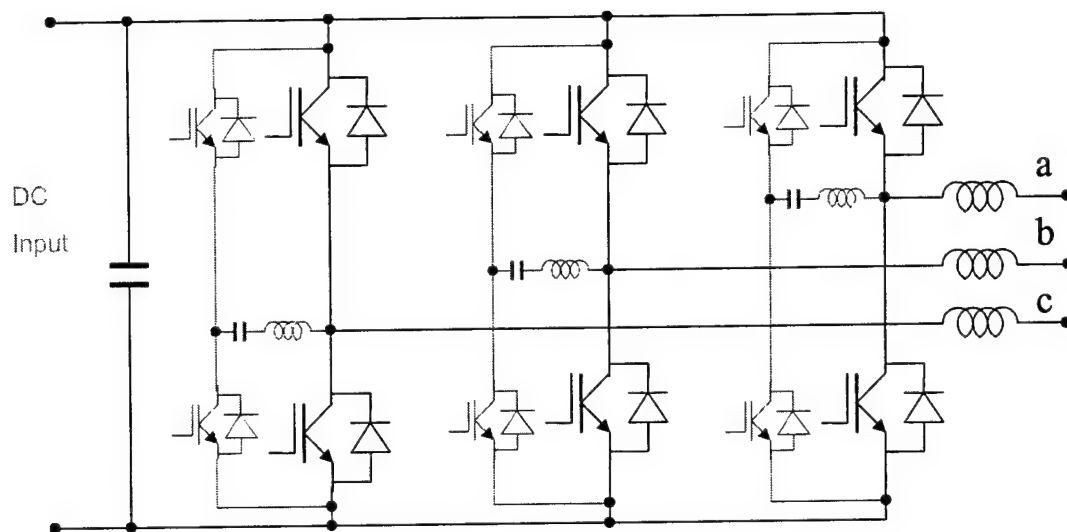


Figure 8-8. Circuit diagram for inverter mode test.

8.4.2 SVM schemes

For this kind of three-phase converter, it is a common practice to use a SVM to generate the gate signals. The SVM algorithm is the core part of this digital controller, for both the DSP and EPLD programming. The timing of the auxiliary switch gate signals for the soft switching also relies on SVM.

There are many SVM schemes available. A lot of literature has been published on the topic. For this high-power application, wide control bandwidth and high performance are desired. Thus, a SVM with high sampling frequency, low switching loss and minimal circulating energy are necessary. The evolution diagram of this SVM from the conventional low total harmonic distortion (THD) SVM is shown in Figure 8-9.

Fifty percent switching loss reduction and doubled sampling frequency have been achieved. The same SVM scheme is used for both the inverter mode and the rectifier mode. Another benefit of this SVM is the soft-switching operation. It can reduce the RMS current in the resonant tank to about 19% from the test measurement compared with the DC-DC result. The problem posed in the single PEBB module high power tests is solved in three-phase tests.

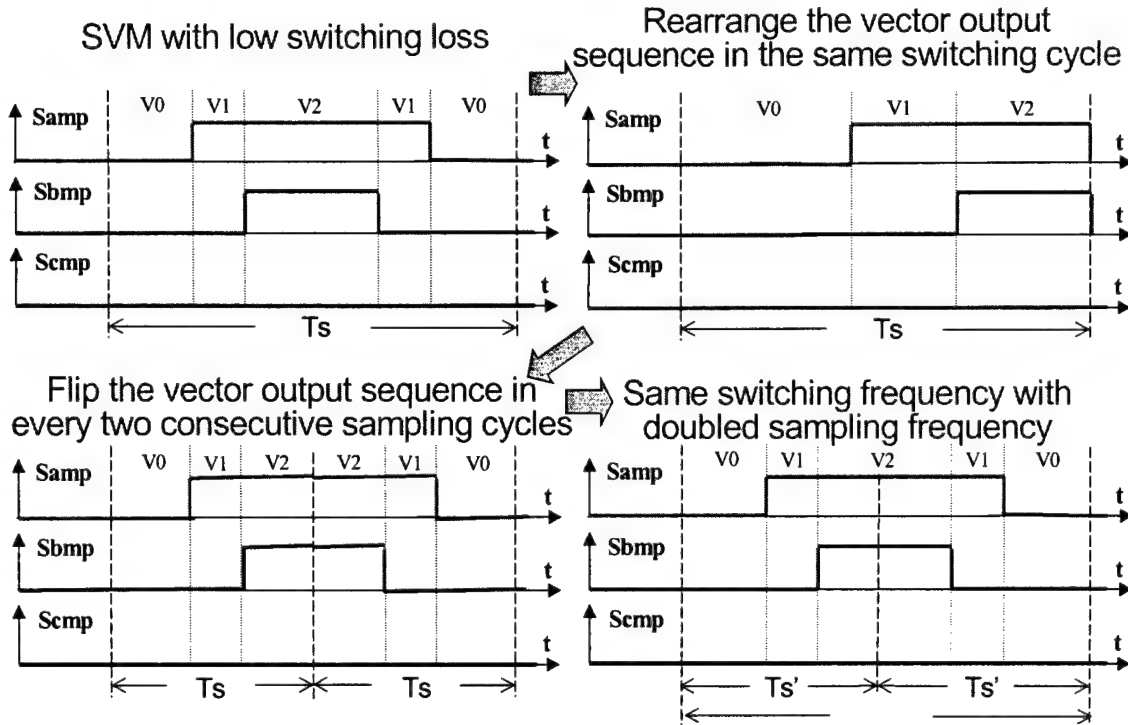


Figure 8-9. Evolution diagram of the proposed SVM scheme.

The main reason for the reduced resonant tank current is that the proposed SVM can save one-third switching events in every line cycle for each phase. Therefore the resonant tank is deactivated during that period of time when the main IGBT does not switch. Furthermore, since the phase with the highest current does not switch, the peak current in resonant tanks also can be designed smaller than in DC-DC applications. About 15% reduction of the peak switching current is reached, which can lead to the further reduction of resonant tank RMS current from the design point of view. Apparently, reducing the peak resonant current can further relieve the electrical and thermal stress on the soft-switching components.

The inverter mode with soft switching tests completed most of the tests for the digital controller under high power, not only the SVM scheme implementation and the auxiliary switch pulse generation, but also the sensor feedback channel and the protection infrastructure for the converter and other peripherals.

8.4.3 Noise issues

Noise issues emerge under high voltage and high power level. The fault signals from the gate drive boards incorporate very high-level noise. It seems that the low pass filters in the circuitry cannot reject the noise under the three-phase high voltage tests. It is reasonable for this three-phase PWM converter topology because the voltage level shift is higher than in its DC-DC counterpart. The noisy fault signals often trigger the protection of the controller erroneously when the DC bus voltage is close to 700V. Since the noise occurs in the form of narrow pulses associated with the switching actions, and the noise pulse is different from the real protection signals, a digital filter is added in the EPLD design to keep the noise away from the controller. The noise immunity of the digital controller is considerably improved after the digital filter is added.

8.4.4 High power test results in inverter mode

The power level in the inverter mode tests is pushed up to 70kW with 800V DC bus voltage. One of the test waveform is shown in Figure 8-10. Channel 2 and 4 are output phase currents (100A/div). Channel 1 is the voltage across a main IGBT switch. Channel 3 is the resonant tank current, which indicates the soft-switching operation. Obviously, the soft-switching operation is only activated when the main IGBT switch is switching.

The test power level is limited to the maximal power that the DC power supply available can deliver without any problem. The reliability of the power stage and basic functions of the controller are tentatively proven by the high power test.

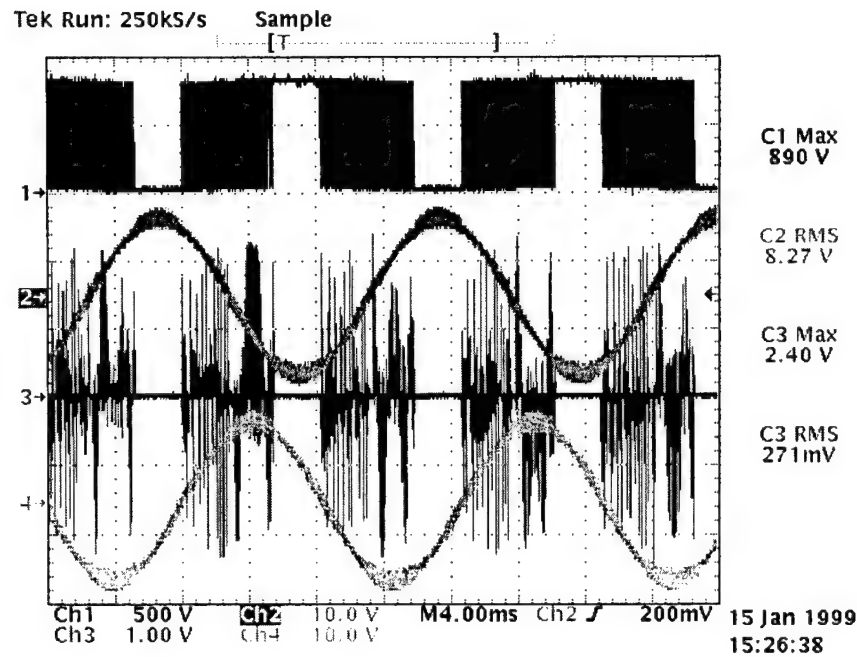


Figure 8-10. Inverter test waveforms at 70kW with ZCT soft switching.

8.5 PFC Rectifier Mode Test

8.5.1 Test setup for rectifier mode operation

The rectifier mode test is conducted after the inverter mode test. The test circuit configuration is shown in Figure 8-11.

During this test stage, the control loop has to be closed. There are two loops that need to be closed in this rectifier. One of them is the current feedback loop, which has fast dynamic. It is used to achieve the sinusoidal (input) phase current as well as power factor correction. The other one is the voltage loop, which has a relatively slow dynamic. This voltage loop is used to regulate the DC bus voltage. In the cascade control scheme of this rectifier, the current loop is used as the inner loop and the voltage loop as the outer loop. The voltage loop is based on the well-designed current loop. For multiple-loop system debugging, the inner loop is closed at first while the outer loop is open.

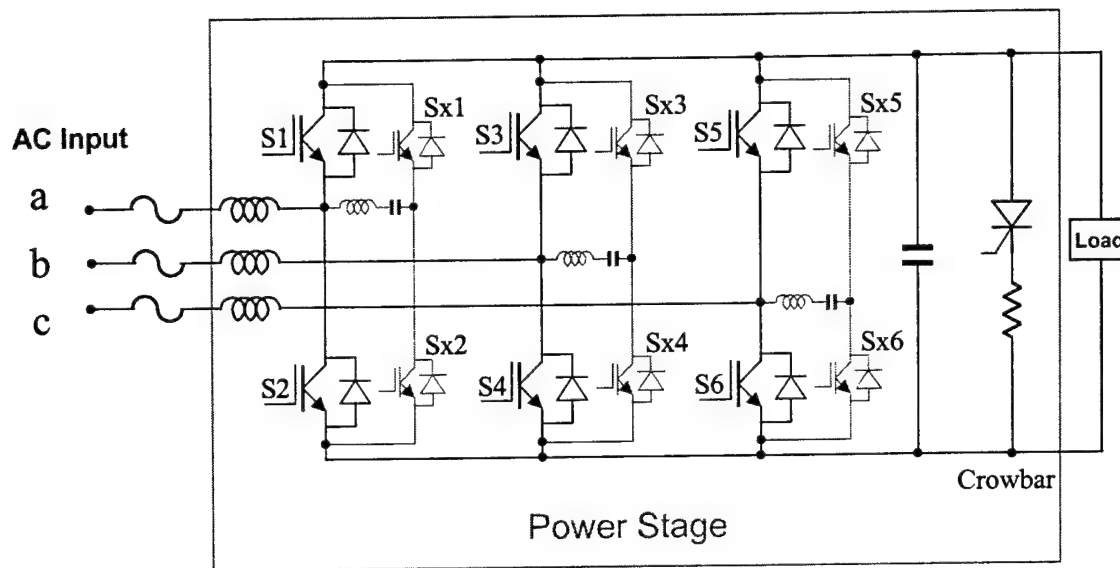


Figure 8-11. Circuit configuration for rectifier mode test.

8.5.2 Crowbar for over-voltage protection

In this boost rectifier, one of the most important protections is the DC bus over-voltage protection. DC bus over voltage will destroy the switches connected to the bus and will cause damage to the other converter systems in the test bed as well. Due to the existence of the bulk capacitors across the DC bus and limited input phase current, it is impossible for the DC bus to build a harmful over-voltage in a few switching cycles. Therefore, it is fast enough for the controller to respond by using the DC bus sensor information. This information is also used for voltage loop control.

However, in some extreme cases, the controller may not work as it is supposed to. The DC bus voltage may exceed the safe operating region for both the active switch and the passive components such as DC link capacitors. The high-level protection mechanism independent from the digital controller has to be added. In this converter, a crow bar is put across the DC bus, which will monitor the DC bus voltage so that it can be prevented from building up to a dangerous level. The threshold is set to 1070V; over this limit, the crow bar will take action. The semiconductor fuses will blow out to cut off the input power. The crow bar will consume energy stored in the DC link capacitors. The test waveforms in Figure 8-12 show the effectiveness of this mechanism.

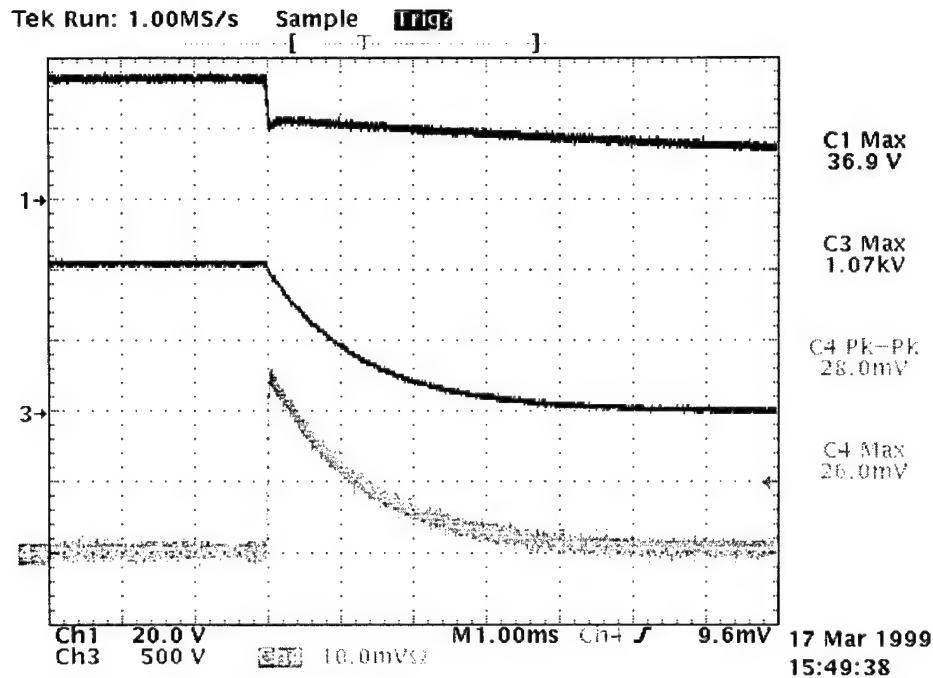


Figure 8-12. Test waveforms for the crowbar.

In Figure 8-12, Channel 3 is the DC bus voltage, and channel 4 (200A/div) is the current flowing into the crowbar. The peak current in the crowbar is 520A.

8.5.3 Controller design

The control parameters for the PWM boost rectifier are designed using the small signal model in SABER simulation software. The switch model in SABER verifies the control parameters. From simulation results, the gain of the current loop increases along with the DC bus voltage. In the rectifier mode tests with the voltage loop open, the method used to increase the power level involves cranking up the input voltage while keeping the input phase current constant. The closed loop keeps the input phase current at the desired level as long as the converter is stable. Therefore, the current regulator has to be designed to be stable under the highest possible DC output voltage when the safety margin is the least, in a small-signal sense. Of course, gain-scheduling techniques can be applied to achieve good performance for the entire DC output voltage range. Since it is just a test for the PI regulator and power stage under rectifier mode, we do not want to further complicate the controller.

Another technique that has to be employed in the controller design is the soft start-up for the input phase current. Due to the high power level this three-phase PWM rectifier has to be tested up to, the input phase current command has to be set to the value for the rated output power level. It is about 120A for 100kW output power at the rated input line-to-line voltage (480V AC). Without a very low current command at the very beginning or other current limiting means, the current loop regulator will saturate during the start-up transition. The inherent limit of the current regulator to the phase current will not be there. High in-rush current may occur during the start-up transition, which could cause saturation of the boost inductor. Further damage to the power stage may happen due to the saturation of the inductor. The high in-rush current can also lead to the failure of the DC bulk capacitors because they have not been charged before the start up. It is possible for the charging current to go beyond the capability of the capacitors without any limit on the input currents. From the above analysis, the soft start-up for the input phase current has to be implemented for the test.

This functional block is implemented in DSP code. The starting value, end value, step change and time delay for each step change can be easily set in the program. The actual start-up phase current can be limited within a few amperes.

8.5.4 Test waveforms for the PWM boost rectifier mode

Since the SABER simulation circuit was made as close to the test setup as possible, the design parameters for the simulation were used in the digital controller. The experimental waveforms except with the current loop closed under different DC bus voltages are shown in Figure 8-13.

In Figure 8-13, channel 1 is the input phase voltage. Channel 2 is the input phase current (50A/div). Channel 4 is the corresponding resonant tank current. The soft-switching function is disabled at the zero crossing of the phase current to achieve better total converter efficiency.

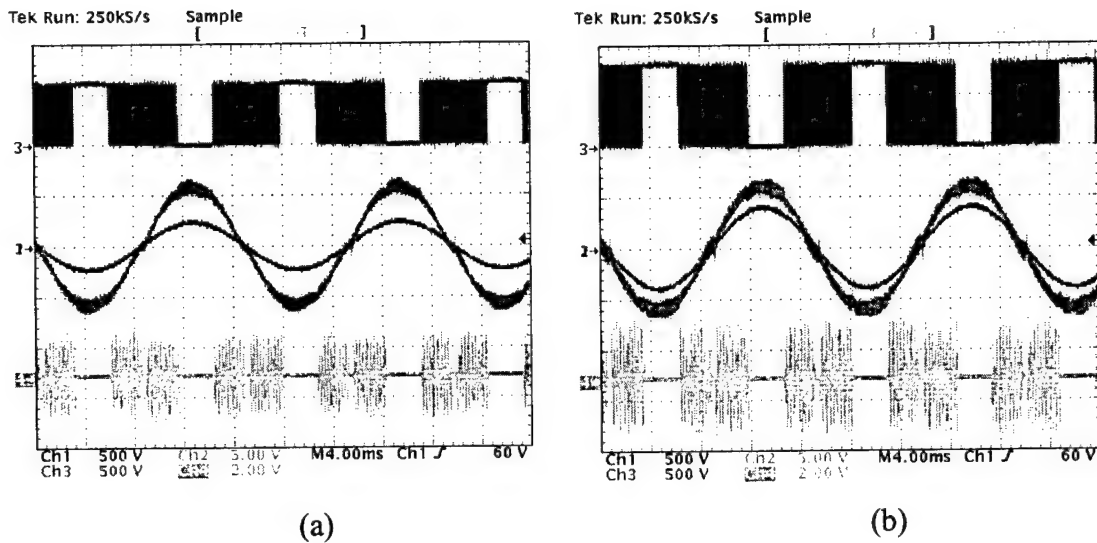


Figure 8-13. Experimental waveforms for rectifier mode under different DC bus voltages.
(a) 600V; (b) 800V.

The power factor correction and sinusoidal phase current waveform depend heavily upon the phase angle information of the input line-to-line voltage. To align the current in phase with voltage for each phase is called synchronization. In this PFC rectifier, the zero crossing detection technique is used. Due to the high frequency, high voltage current switching of the converter, the line-to-line voltage may have strong noise. Especially at zero crossing, the noise level may overwhelm the actual voltage signal. The filtering stage has to be carefully designed. From the test result, the synchronization is well implemented. It works well under all the tests regardless of the voltage and current levels. Otherwise, the phase locked loop (PLL) technique has to be applied. Of course, this will add extra hardware into the controller.

The voltage loop is closed and tested after the current loop is successfully closed. Figure 8-14 is the test waveform under 800V DC voltage output. In Figure 8-14, V_a is the phase voltage, and I_a is the phase current (50A/div). The output power is over 50kW.

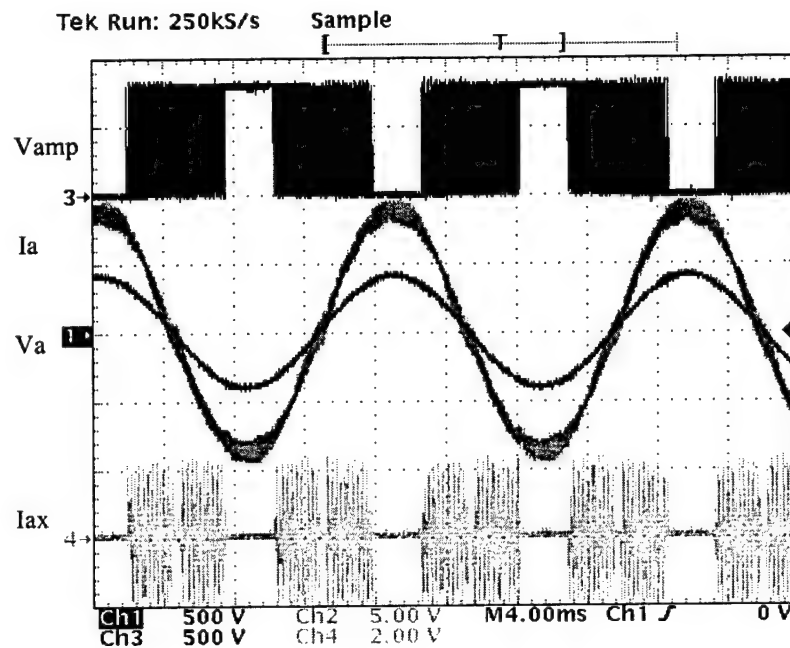


Figure 8-14. Experimental waveforms with two loops closed under 800V.

As is stated in the inverter test section, we choose a SVM scheme to achieve doubled sampling frequency while keeping the same switching frequency. In the rectifier mode tests, 20kHz switching frequency is applied. The 40kHz sampling frequency is reached. Therefore, the control bandwidth for the current loop can be easily pushed up to 2 kHz. The bandwidth of the voltage loop also can be pushed to 500 Hz. The wide loop bandwidth ensures a tightly regulated DC bus of the distributed power system for the system integration.

8.6 DSP Control Program For The Plug And Play

Plug and play (PnP) is a concept based on PEBB but taken a step further. Power electronics systems built with the PnP concept allow the interchange among different PEBB modules, which means the PEBB modules can have different topologies (such as different soft-switching topologies) as long as the PEBB modules can fulfill the same functionalities required by the system. Each PEBB module has standard hardware and software interface. A low-level controller is integrated into each PEBB module. This controller is called a hardware manager (HWM). The PnP concept is also applied to the controller of the converter. In other words, the controllers are also interchangeable. Every PnP controller is developed for a specific application. This kind of PnP controller

is called an application manager. Therefore, the conventional converter is divided into two parts, one part is one or more PEBB modules with an HWM, and another part is the application manager. The control information is transferred between these separate parts by optical fibers. The application managers can be controlled by a system-level controller via high-speed data link. The wide bandwidth of the fiber optic cables can enable the high-speed communication between the separate parts. The optical fibers can construct power electronics system networks in the future. A preliminary demonstration system that consists of two PnP inverters is shown in Figure 8-15. The two PnP inverters have different soft-switching topologies, so their HWMs are different too. However, just by exchanging fiber optic cables, different inverters can replace each other.

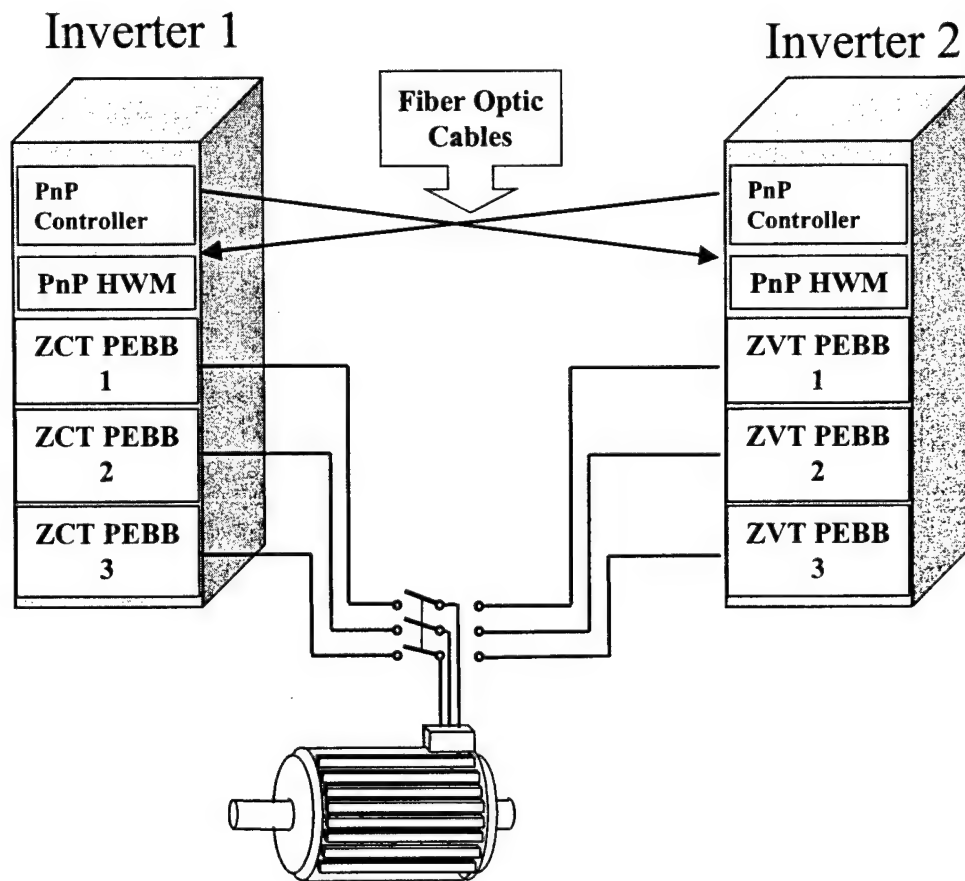


Figure 8-15. A plug and play demonstration system.

With the PnP concept, a three-phase converter can be configured as a voltage source inverter for the motor drive or as a boost rectifier for power factor correction. To demonstrate this concept, a DSP program for the PnP show in Chicago (PCIM'99) is

developed. This program can be used to control a butterfly valve driven by an induction motor or for other induction motor applications. For the butterfly valve, the information about the limit switches being open or closed should be sensed by the controller. The controller should control the direction of rotation and the start-up/stop of the motor. Soft start and variable frequency operation of the butterfly valve control is implemented to achieve high performance. The simplified main DSP routine for the butterfly valve control is shown as Figure 8-16.

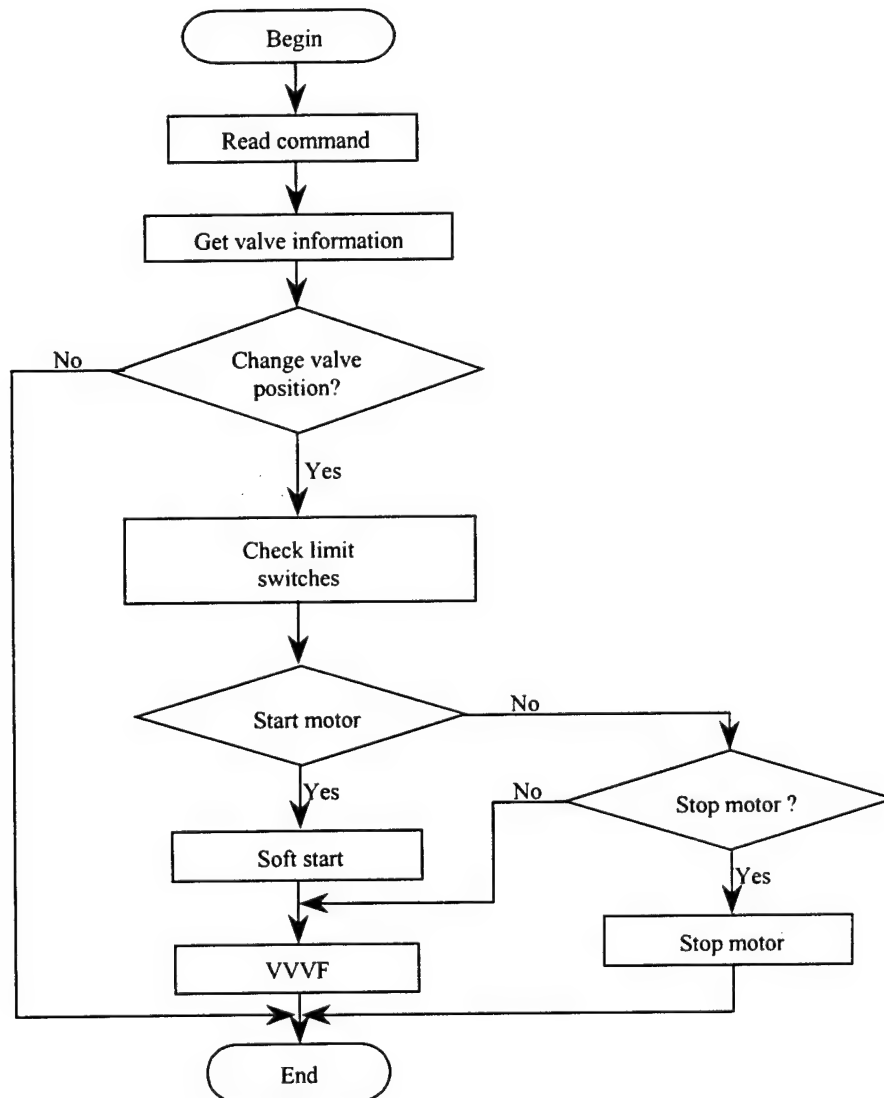


Figure 8-16. Flow chart of the DSP program for butterfly valve control.

8.7 Low-Frequency Harmonics Caused By PWM And Their Elimination

Although the operation of the AC-side commutated soft-switching technique adopted here should have negligible effect on the rectifier's operation in terms of low frequency, significant low-frequency harmonics have been observed in this rectifier by test and simulation results. Figure 8-17 shows the simulated input phase current of this rectifier with an ideal three-phase AC source and an ideal resistive load.

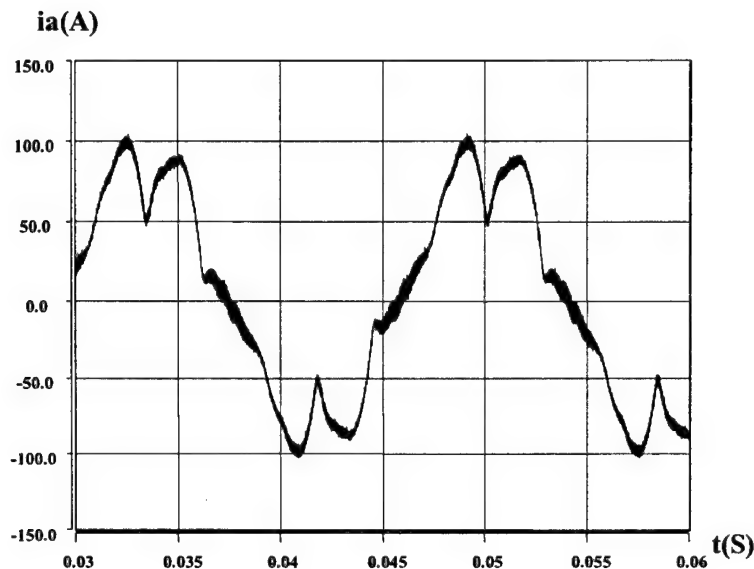


Figure 8-17. Phase A input current waveform of the IZCT soft-switched boost rectifier.

The harmonic spectrum is shown in Figure 8-18. The low-order harmonics are comparable to the fundamental frequency component. The total harmonic distortion (THD), mainly low-frequency harmonics, is about 21.4%. Low-frequency harmonics generated by the rectifier appear at the DC output side in the form of low-frequency DC voltage ripple, as shown in Figure 8-19.

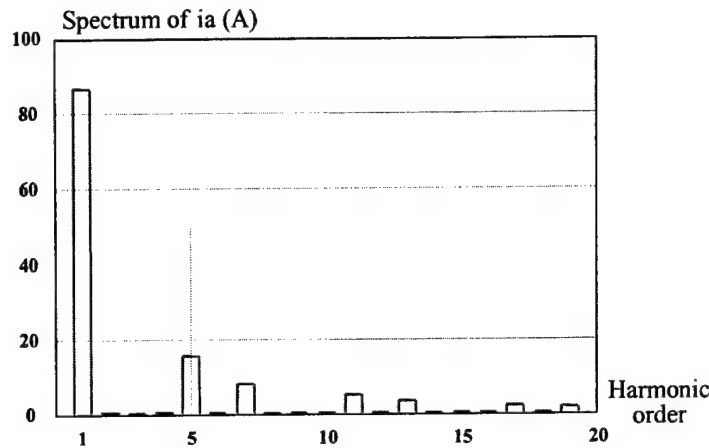


Figure 8-18. Spectrum of phase current.

Low-frequency harmonics is an important issue in power conversion and power quality areas. Apart from their harmful effects on the AC source (such as generator sets), strong low-frequency harmonics can limit the rectifier's control bandwidth to such an extent that the rectifier cannot tightly regulate the DC bus. On the other hand, low-frequency DC voltage ripple may cause oscillation of the whole DC distributed power system. Moreover, low-frequency harmonics are more difficult to eliminate than high-frequency ones. In order to filter out the low-frequency harmonics, bulky low-pass filters have to be added at both the input and output sides of the rectifier. As a result, the volume and cost of the rectifier will increase significantly. Therefore, it is extremely important to investigate how these low-frequency harmonics are generated and find ways to remove them from the practical perspective.

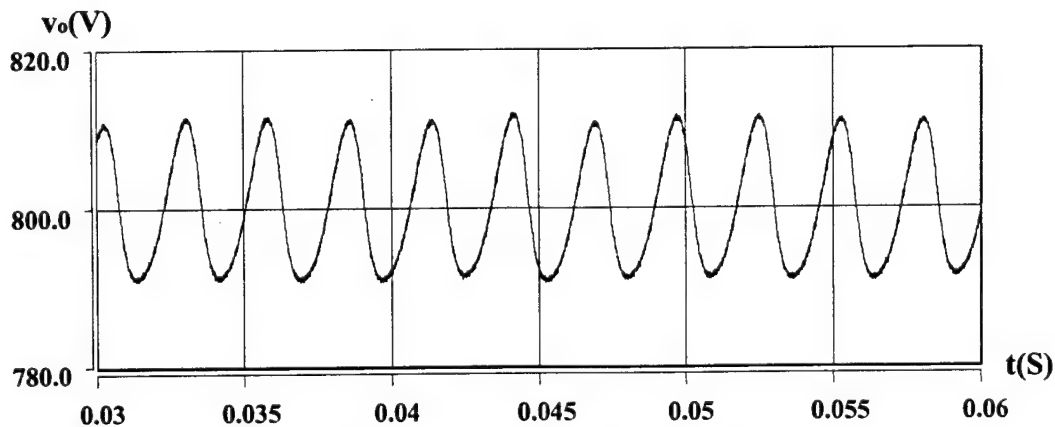


Figure 8-19. DC voltage ripple at the rectifier output.

Three major causes have been identified for low-frequency harmonics caused by PWM: pulse width limits, an improper SVM scheme and dead time. The first cause is only related to soft switching techniques, while the other two reasons may also exist in three-phase hard switching converters. These causes will be illustrated in the following sections. Solutions and correction techniques to achieve clean rectifier input current are also provided.

8.7.1 Pulse width limits in soft-switched PWM converters

Pulse width limits have to be set for three-phase soft-switched PWM converters. Soft-switching techniques utilize high-frequency resonant circuit to achieve favorable switching transitions for power switches and diodes in PWM converters. The whole resonant process is normally much longer than the switching transition itself. In order to avoid the malfunction of the resonant tank due to the overlap between the consecutive resonant cycles, pulse width limits must be set for the main switch gate signals.

In this ZCT soft-switched PWM converter, the same resonant tank operates twice for every switching cycle. As illustrated in Figure 8-20, the pulse width T_w of the main switch gate signals has to be limited by the equation (1).

$$T_{lim} \leq T_w \leq T_s - T_{lim} \quad (1)$$

where T_s is the switching period, and the minimal pulse width limit $T_{lim} = \max(t_1 + t_4, t_2 + t_3)$.

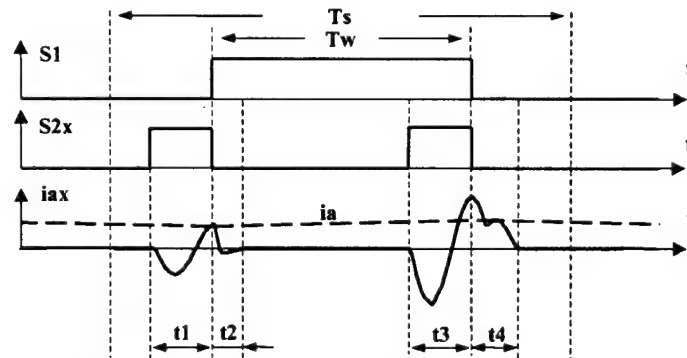


Figure 8-20. ZCT soft-switching operation waveforms.

The equation (1) is not applied when the duty cycle equals 0 or 1 because the soft switching is not activated under this circumstance. In the presented rectifier, the

switching frequency is 20kHz. To obtain satisfactory soft-switching operation, the resonant period is about 4 μ s. The minimal pulse width limit T_{lim} for the main switch gate signals is 6 μ s, and the maximal pulse width limit is 44 μ s. Therefore, the effective switch duty cycle ranges from 0.12 to 0.88. In this rectifier, the switch duty cycle is the same as the phase duty cycle. We are going to use the term phase duty cycle in the following discussion.

The impact of the duty cycle loss on the steady state operation of three-phase PWM converters is not as straightforward as on their DC-DC counterparts. First, the duty cycle for each phase in a three-phase PWM converter is changing in a line cycle. Second, the phase duty cycle depends on modulation strategies even under the same operating point (same modulation index). In this paper, we call the method of choosing zero and non-zero vectors a modulation strategy. An SVM scheme refers to a modulation strategy with a determined vector sequence. To investigate the impact of the duty cycle loss on the PWM rectifier, we compute the modulation index for the given operating point by equation (2).

$$M = \sqrt{\frac{3}{2}} \cdot V_{ll_rms} / V_o \quad (2)$$

where V_o is the DC bus voltage, and V_{ll_rms} is the RMS value of the input line-to-line voltage.

The modulation index at the operating point is 0.734 from equation (2) for this rectifier (the specifications are listed in the appendix). For the sake of simplification, a commonly used modulation strategy with the two zero vectors applied evenly will be analyzed as an example. The phase duty cycle d_a for this modulation strategy is shown in Fig. 1.21. The pulse width limits, in the form of the duty cycle, are indicated by the dashed line D_{max} and D_{min} in Figure 8-21. The shaded areas show when the phase duty cycle command is limited. Even if we use one SVM scheme of this modulation strategy, which has the least high-frequency harmonics due to the symmetrical arrangement of the vectors [5-7], the duty cycle limits still lead to the heavily distorted input current as shown in Fig.

1.17. The maximal modulation index M without any distortion for this modulation strategy is given by equation (3).

$$M \leq \sqrt{3}/2 \cdot (1 - 2 \cdot T_{lim}) \quad (3)$$

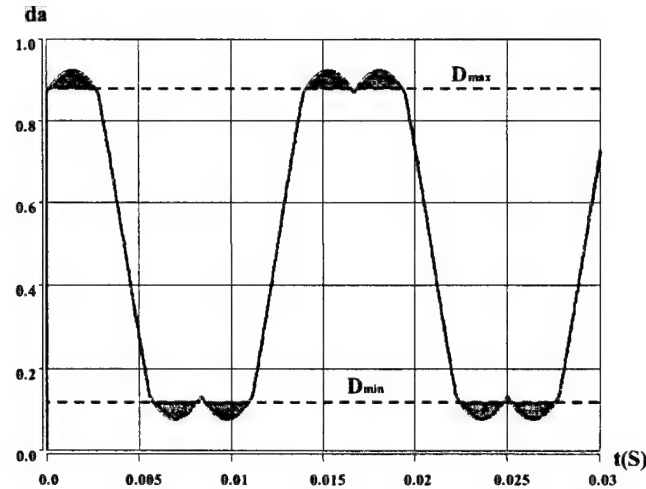


Figure 8-21. Continuous phase duty cycle pattern.

From equation (2), the maximum M with the pulse width limits is 0.658. This maximum M means the command duty cycle is limited by the pulse width limits under the specified operating point. Also, this modulation strategy is only suitable for the soft-switched PWM converters with low and medium modulation indices.

As mentioned at the beginning of this paper, PWM boost rectifiers normally have a high modulation index. It is necessary to find a modulation strategy suitable for high modulation index applications. The proposed solution is to utilize the freedom of selecting the zero vectors to shape the phase duty cycle pattern. By properly choosing the zero vectors, the phase duty cycle pattern for the same operating point is changed to what is shown in Figure 8-22. Here, the shaded areas denote the discontinuity of the new duty cycle pattern. It is evident that this discontinuous modulation strategy avoids the pulse width limits in the presented rectifier. This discontinuous modulation strategy is the same strategy that can reduce the switching loss by 50% under the unity power factor [8]. The modulation index range without any distortion for this modulation strategy is determined by equation (4).

$$\sqrt{3} \cdot T_{lmt} / T_s \leq M \leq \sqrt{3} / 2 \cdot (1 - T_{lmt} / T_s) \quad (4)$$

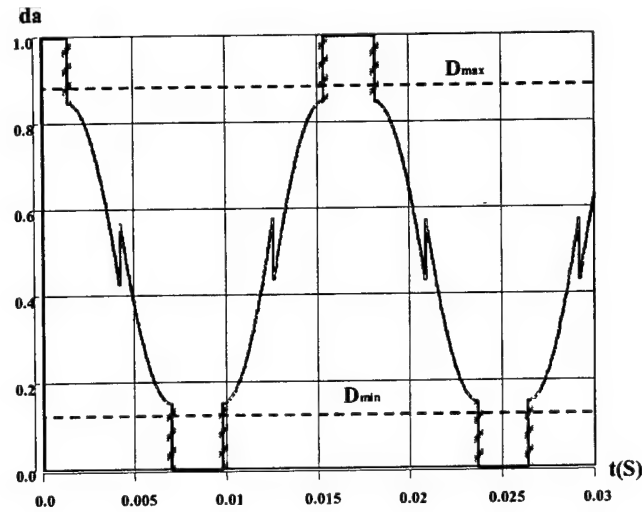


Figure 8-22. Discontinuous phase duty cycle pattern.

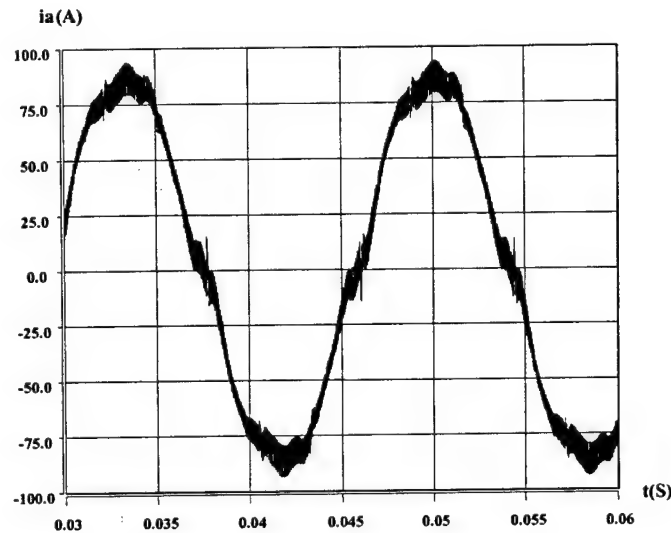


Figure 8-23. Simulated input current with the effect of pulse width limits avoided.

Equation (4) gives the $M_{min} = 0.207$ and $M_{max} = 0.762$. Therefore the modulation index at the specified operating point is not affected by the pulse width limits. As shown in Figure 8-23, the input phase current waveform is significantly improved by the discontinuous modulation strategy. The distortion left in the input current waveform of Figure 8-23 is owing to the other two causes.

8.7.2 Improper space vector modulation scheme and its correction

An improper SVM scheme is identified as another cause of the low-frequency harmonics in the PWM rectifier. SVM is a prevailing technique in controlling three-phase PWM converters. There are numerous SVM schemes. They can be divided into two classes: symmetrical and asymmetrical schemes. An asymmetrical scheme is shown in Figure 8-24a. NZ1 and NZ2 are the two non-zero vectors selected to synthesize the reference vector. Z1 is one of the zero vectors. A symmetrical is as shown in Figure 8-24b. As described in the literature [5-7], different SVM schemes can have different high-frequency harmonics. The asymmetrical schemes are easy to implement but have more high-frequency harmonics. High-frequency harmonics are relatively easy to get rid of by adding a small EMI filter, while low-frequency harmonics are much more difficult to suppress.

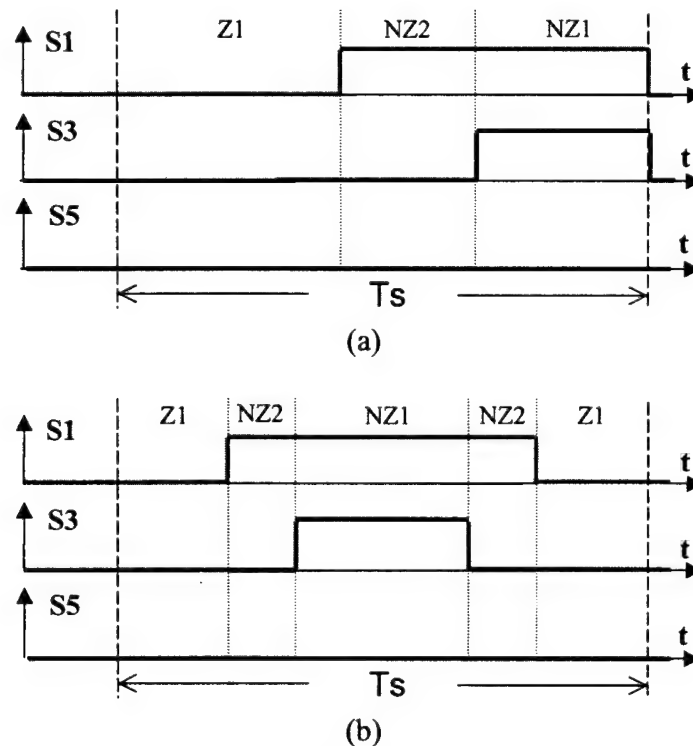


Figure 8-24. SVM scheme examples: (a) asymmetrical scheme; (b) symmetrical scheme.

Nevertheless, it is found in this research that an improper SVM scheme also can cause pronounced low-frequency harmonics. An improper SVM scheme is shown in Figure 8-25. Z1 and Z2 are the two zero vectors available in a three-phase PWM converter. To

achieve the phase with maximum current not switching, the two zero vectors are applied alternatively. The sequence of the vectors is arranged in a way to minimize the switching loss. However, the low-frequency harmonics resulted, as shown in Figure 8-26.

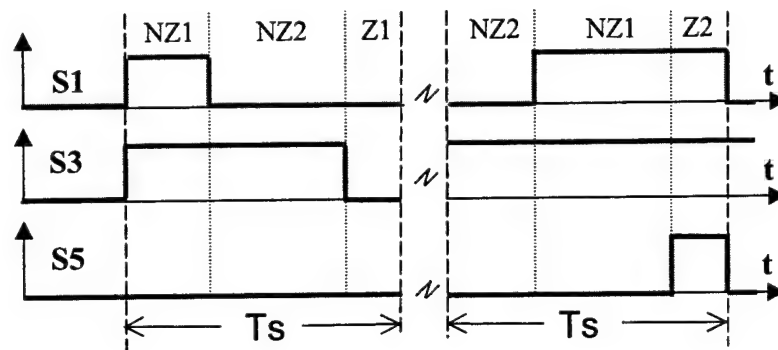


Figure 8-25. An improper SVM scheme.

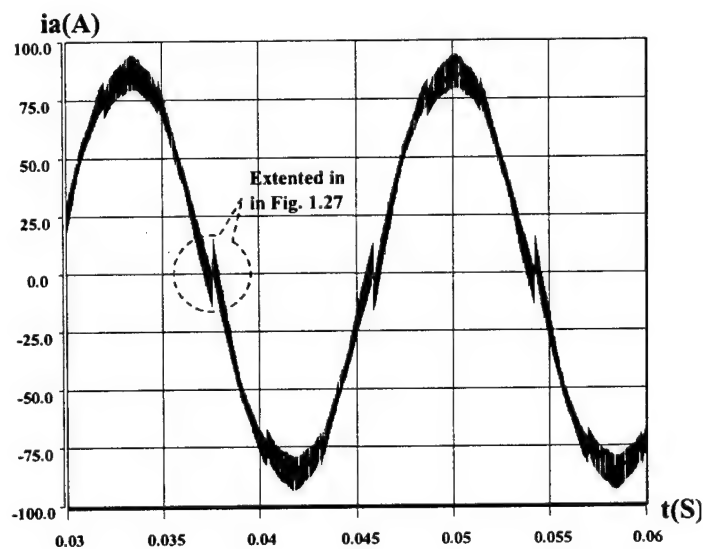


Figure 8-26. Distorted input phase current due to the improper SVM scheme.

The reason for the low-frequency harmonics can be illustrated in Figure 8-27 by the extended view of the phase current waveform at the zero crossing where the distortion occurs. The sequence of the non-zero vectors changes near the zero crossing to minimize the switching actions. This change leads the average phase current of a switching cycle to shift by the magnitude of the input inductor current ripple.

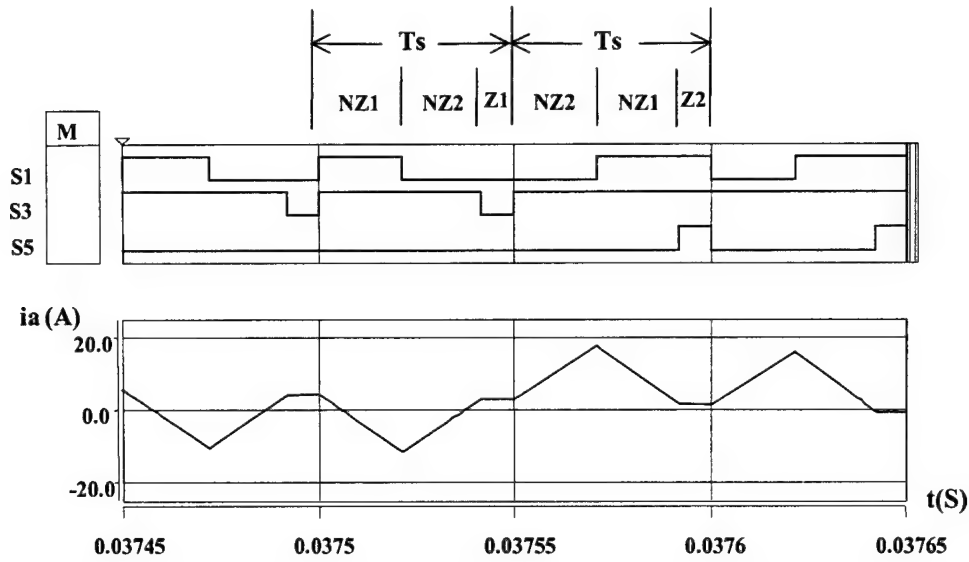


Figure 8-27. Detail of phase current at zero-crossing and associated main switch gate signals.

The solution is to rearrange the sequence of the non-zero vectors, as shown in Figure 8-24b. This scheme is referred to as symmetrical 60° clamping SVM [9]. The detail of the phase current waveform at the zero crossing with this scheme is shown in Figure 8-28. Since the average current in a switching cycle is roughly equal to zero, smooth transition is achieved at the zero crossing points. After this cause is corrected, the input current waveform is changed to the one in Figure 8-29.

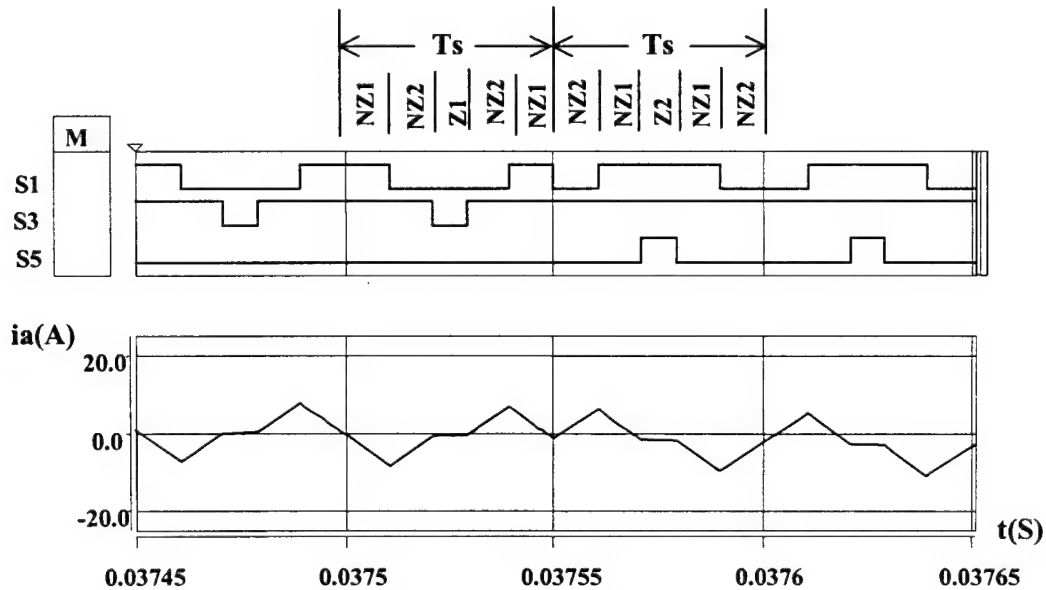


Figure 8-28. Corrected input phase current at the zero-crossing.

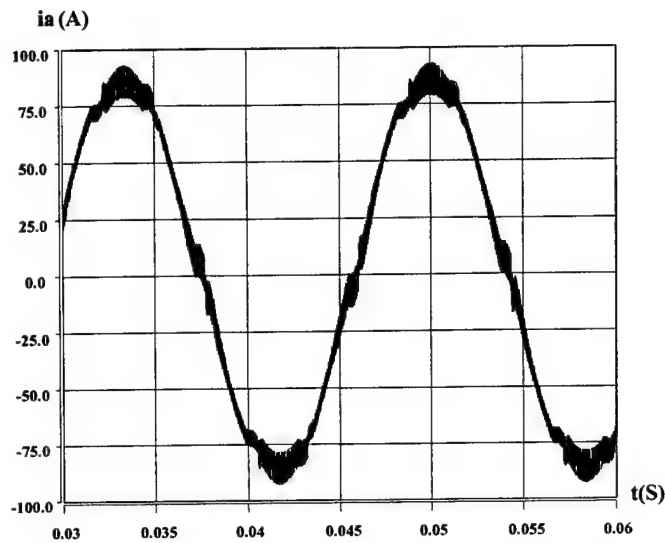


Figure 8-29. Phase current waveform with dead time.

8.7.3 Dead time and its compensation

The third major cause for low-frequency harmonics is dead time. Dead time is inserted into the gate signals of the complementary main switches to prevent a short circuit of the DC bus. The dead time is $2\mu\text{s}$ for the presented rectifier.

The dead time compensation methods are widely investigated for the voltage source PWM inverters [10-12]. Most of the compensation techniques fall into two categories. One is based on an average value theory [10]. The lost volt-seconds are averaged over an entire cycle and added to the voltage command. In the other category, dead time compensation is realized for each PWM switching cycle [11,12]. These techniques can get better performance because the compensation has much less phase lag. The key factor in obtaining good compensation is accurate polarity information for each phase current.

Since we can regard PWM boost rectifiers as voltage source PWM inverters with reversed power flow, the compensation techniques proposed for inverters can be applied to rectifiers. Additionally, PWM rectifiers have to use current closed-loop control to achieve sinusoidal input and power factor correction. It is possible to obtain accurate phase current information in the rectifiers. Dead time compensation can be conducted in every switching cycle.

The suggested compensation method is to extend the pulse width of the main switches carrying current by the amount of dead time, as shown in Figure 8-30. S_a^* is the command gate signal for phase A. Here, we assume the top switch S1 is switching current. Thus, we do not care about the gate signal for S2. We extend S_{ad}^* by the length of the dead time so that S1 has the correct pulse width after the dead time processing circuit. The actual gate signal for phase A is shown as S_a , which does not have any duty cycle loss except a dead time delay added.

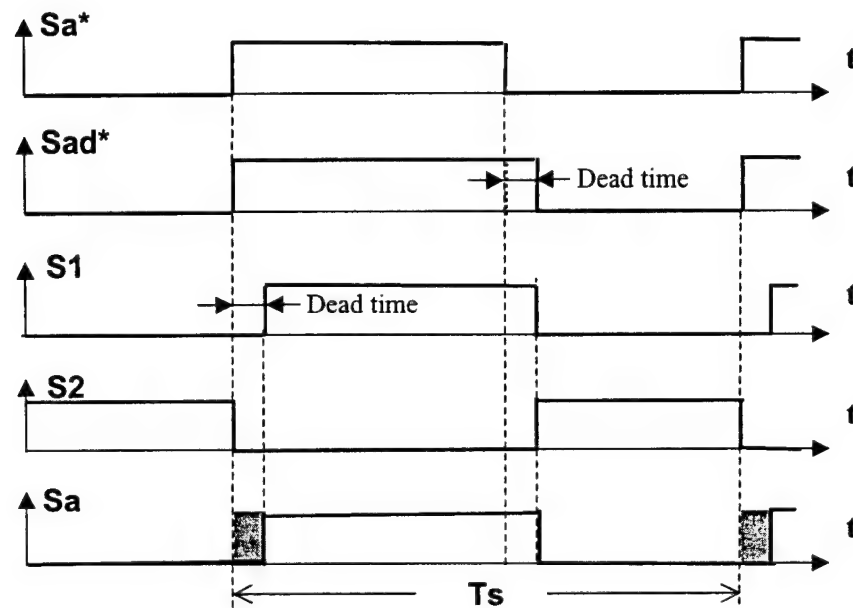


Figure 8-30. Dead time compensation scheme.

Phase A current waveform with the dead time compensation is shown in Figure 8-31. Clean phase current waveform is achieved after all these causes associated with the PWM techniques are corrected. The spectrum of the low-frequency harmonics in the phase current is shown in Figure 8-32. Apparently, the low-frequency harmonics are almost eliminated. The THD for this waveform is about 0.37%. With these correction techniques applied, the experimental waveforms are shown in Figure 8-14.

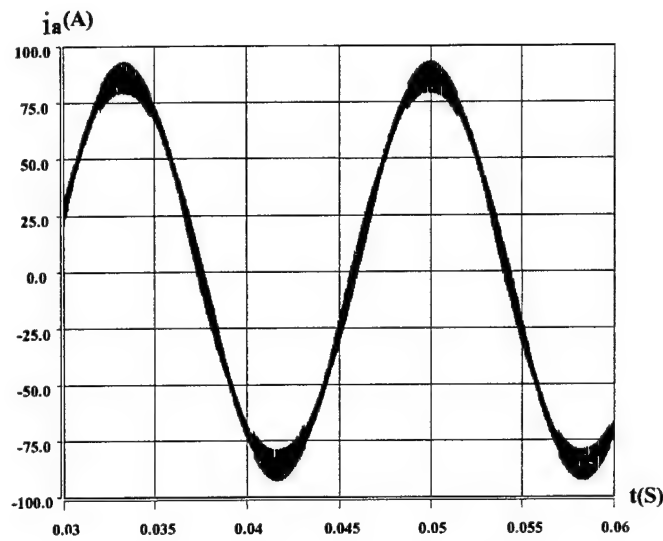


Figure 8-31. Phase current waveform without dead time.

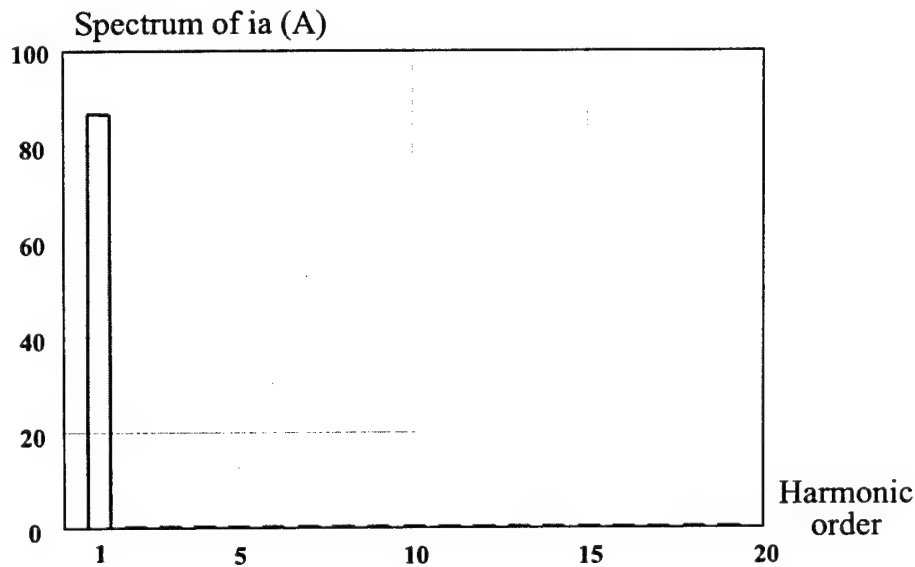


Figure 8-32. Spectrum of the phase current after correction.

8.8 Summary and Future Work

So far, the soft-switched DC bus regulator has been successfully tested under high power level with 20kHz switching frequency and 40kHz sampling frequency. Both of the current and voltage feedback loops are closed. The maximum power level for the power stage is tested up to 70kW. Major associated issues have been solved in these tests. Therefore, this soft-switched DC bus regulator is ready for the system integration. A

DSP control program is developed for the butterfly valve. Thus, this DC bus regulator can also be configured as a motor drive inverter in a PNP demonstration system.

Several issues are observed in these tests. One of the issues is the low-frequency harmonics caused by the PWM. Three causes have been identified: pulse width limits, an SVM scheme and dead time. This low-frequency harmonics issue is investigated and solved. Another issue is the thermal and electrical stress on the resonant capacitor for the soft switching. Although this issue is basically solved by modulation techniques in three-phase operation, it will be better if we can solve this issue by minimizing the circulating energy. The thermal and electrical issue will become an incentive to either optimize the existing soft-switching technique or look for a better topology.

In the next phase of the research for this DC bus regulator, we will focus on the following topics:

1. System Integration. Intensive system level tests will be conducted under various system configurations. Different loads, such as unbalanced load and nonlinear load will be used. Wide operating ranges and nonlinear natures of the different load converters require advanced control strategy for this source converter. Some nonlinear control strategies might need to be introduced to achieve good performance over the entire operation range.

2. Soft Switching. It is necessary to investigate the impact of the soft switching on the DC bus regulator and possibly the distributed power system.

- a. Further evaluate and improve ZCT soft-switching PEBB performance in the distributed power system.

- b. Optimize the operation of the existing soft-switching technique.

- c. Minimize the high-frequency ripple at the DC output side due to the soft-switching operation.

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Chapter 9 Four-leg Secondary Utility Power Supply Inverter

9.1 Introduction

There are various AC loads such as the three-phase motors on shipboards. For a distributed DC bus power supply system, to provide high quality energy to these AC loads, a high-power, high-performance secondary utility bus is needed. Since the loads may be arbitrary as balanced and/or unbalanced, linear and/or nonlinear, a traditional three-leg three-phase inverter cannot control the load zero-sequence current effects because this inverter does not provide a path for the zero sequence components. Therefore, a return ground is required to deal with the zero sequence component of the load current. Hence, the secondary utility power supply becomes a four-wire system.

There are two ways to implement the return ground: One is connecting it to the midpoint of the split DC link capacitors, that the ground voltage would be clamped at one-half of the DC link voltage, and the three-phase inverter would become three independent single-phase half-bridge inverters. Consequently, the achievable value of a line-to-neutral output voltage is not higher than $0.5V_g$. Due to the inefficient use of the DC voltage, the DC link voltage has to be 15% higher to obtain the same output voltage. Also, because the capacitors receive the ground current directly, unrealistically high DC link capacitance is required to stabilize the DC voltage. Without this stabilizing capacitance, the AC output voltages would be greatly distorted, especially in the case of a highly unbalanced load.

The second approach involves adding a fourth leg as a neutral leg to a conventional three-phase bridge, as shown in Figure 9-1. The ground current caused by an unbalanced (or nonlinear) load flows through the neutral leg, instead of through the DC link capacitor. Since the DC link capacitor now only receives the 2ω -frequency ripple power due to the negative sequence load current, rather than the zero sequence current in the split capacitor scheme, a much smaller dc-link capacitance is needed. A better use of the DC link voltage is very important in high voltage/power applications; because it gives more control headroom, as well as a more reliable and cost effective system.

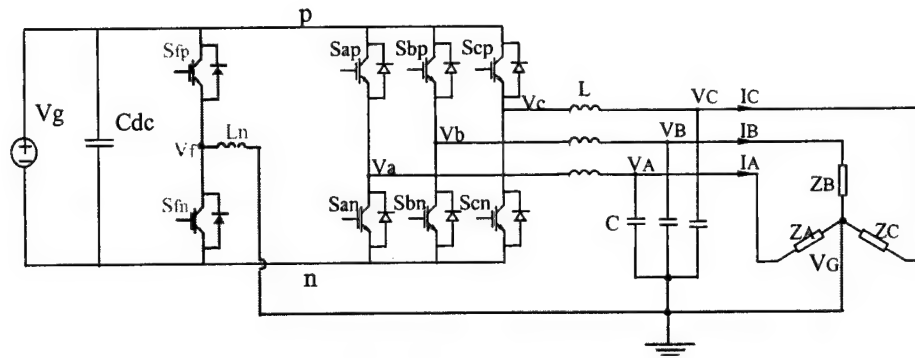


Figure 9-1. Three-phase inverter with a neutral leg.

In this project, a secondary utility power supply subsystem testbed was built based on the PEBB DC distribution power supply system. The goals for this testbed are outlined below:

- Output voltage: 277 Vac (phase-to-ground, rms)
- Output frequency: 60 Hz
- Output voltage THD: < 3% (balanced linear load)
- Output power: 100 kW (three-phase)
- Load power factor range: [-0.8, +0.8]

Also, with this testbed, we want to explore some control and system issues of the four-legged converter subsystem.

9.2 3-D SVM Schemes

9.2.1 Coordinate transformation

The three-phase four-legged inverter system is shown in Figure 9-1. Compared with the conventional three-phase three-legged inverter, the additional leg provides a return path for the load neutral point so that the zero-sequence component can be regulated.

For space vector modulation implementation, we need coordinate transformation. However, instead of the 3/2 transformation in a conventional three-legged inverter, here we use 3/3 transformation; i.e. transform variables in a-b-c coordinates X_{abc} into variables

$X_{\alpha\beta\gamma}$ in three-dimensional orthogonal α - β - γ coordinates by applying the following equation:

$$\begin{bmatrix} X_\alpha \\ X_\beta \\ X_\gamma \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix} \dots\dots\dots (1)$$

In a conventional 3-legged inverter, X_γ is left out due to the assumption of $X_a+X_b+X_c=0$. When the variables in a-b-c coordinates X_{abc} can be mapped into $X_{\alpha\beta}$ in an α - β plane, the SVM becomes two-dimensional, whereas, in a four-legged inverter, due to X_γ , another dimension was added to the space vector. Therefore, the SVM becomes three-dimensional.

Similar to the 3-legged inverter case, we use switching vectors, i.e. ordered sets $[S_a, S_b, S_c, S_f]$ to represent the switch combinations, where $S_a(\text{or } S_b, S_c, S_f) = 'p'$ denotes that the upper switch in phase A(or B, C, Neutral), $S_{ap}(\text{or } S_b, S_c, S_f)$, is closed and $S_a(\text{or } S_b, S_c, S_f) = 'n'$ denotes that the bottom switch in phase A(or B, C, Neutral), $S_{an}(\text{or } S_b, S_c, S_f)$, is closed. The switching vector determines the inverter output voltages $[V_{af}, V_{bf}, V_{cf}]^T$. The spatial positions of the switching vectors in $\alpha\beta\gamma$ orthogonal coordinates can be obtained by applying (1) to converter $[V_{af} \ V_{bf} \ V_{cf}]^T$ into $[V_\alpha \ V_\beta \ V_\gamma]^T$, which is shown in Figure 9-2. There are two zero switching vectors (pppp, nnnn), and 14 non-zero switching vectors. Projection of all switching vectors on the α - β plane forms a hexagon, which is similar to that of a conventional three-legged inverter, shown in Figure 9-3.

9.2.2 3-D SVM schemes with zero vector enabled

The space vectors form six prisms. Each spans a 60-degree region and contains six non-zero vectors and two zero vectors, as shown in Figure 9-2(b). Every three adjacent non-zero vectors and two zero vectors define a tetrahedron, and the reference vector located in this tetrahedron can be synthesized by these five vectors.

There are always six non-zero vectors and two zero vectors available in a prism, as shown in Figure 9-2(b). The possible selections of applied switching vectors are numerous. To eliminate circulating energy and to reduce inductor current ripple, in a conventional three-legged inverter, a six-step operation 2-D SVM, two adjacent non-zero switching vectors and zero switching vectors are used to synthesize the reference voltage vector. Based on the same reasoning, in the 3-D SVM, adjacent vectors also are desired to synthesize the reference vectors. The 60-degree region can be divided into four tetrahedrons, as shown in Figure 9-3.

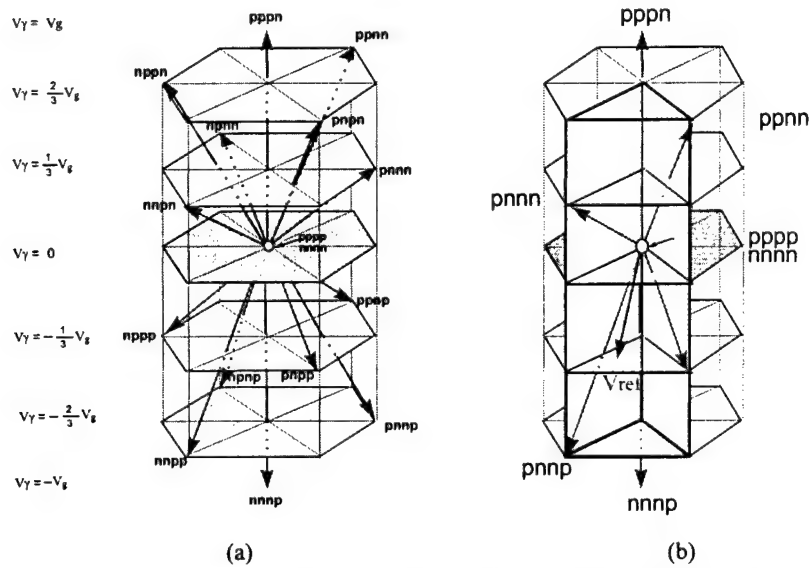


Figure 9-2. (a) Switching vectors of a three-phase inverter with a neutral leg.
(b) Switching vectors in one 60-degree region.

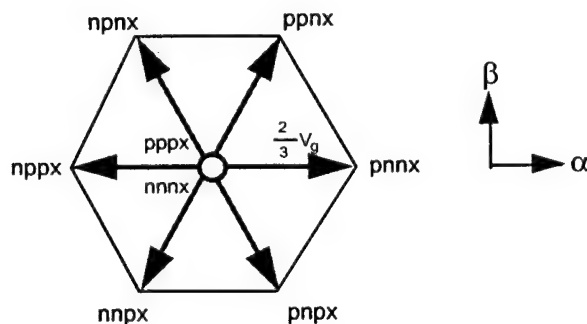


Figure 9-3. Projection of switching vectors on α - β plane.

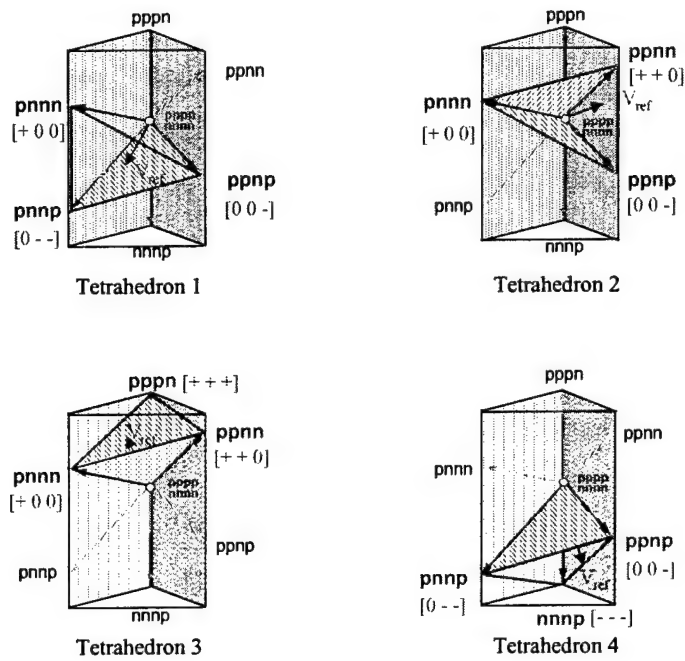
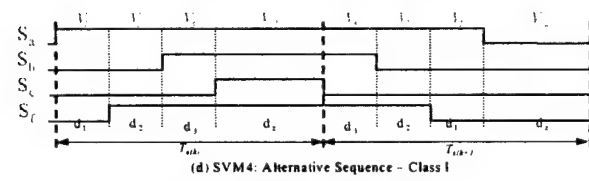
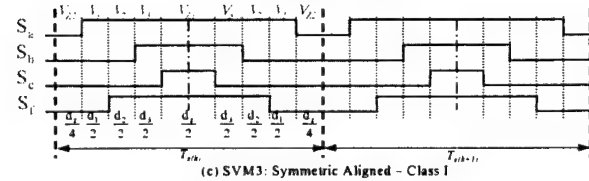
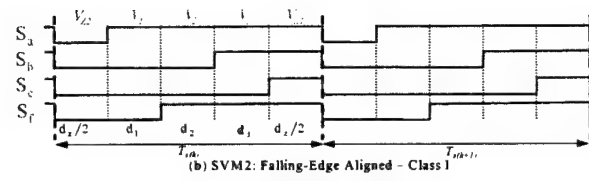
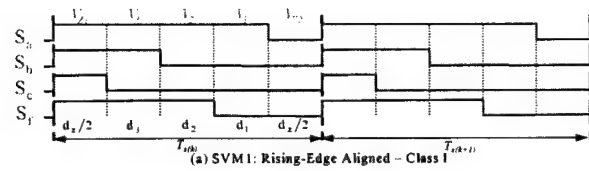


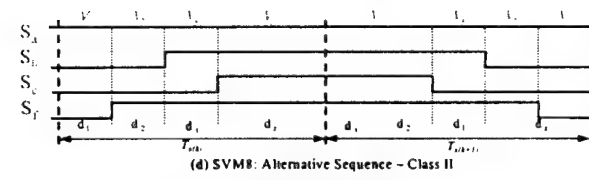
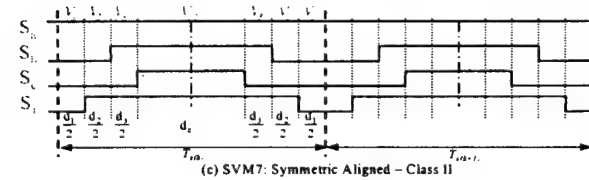
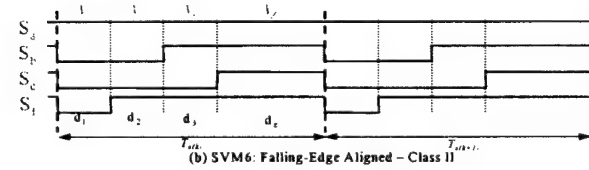
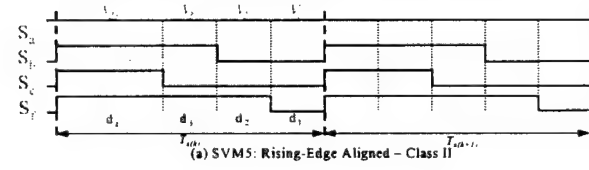
Figure 9-4. Tetrahedrons defined by adjacent vectors(Prism I).

As soon as the space vectors and the corresponding applying duration are determined, the vectors can be applied in different sequences according to different optimization methods. The sequence can be optimized to reduce switching loss by reducing switching actions and by not switching the highest current, or can be optimized to achieve a better voltage THD. The choice of sequencing pattern is a trade-off between switching loss and waveform quality.

Like a two-dimensional SVM, the sequencing schemes for a three-dimensional SVM also can be grouped into two classes. Class I schemes use both two zero vectors, pppp and nnnn, while Class II schemes use only one of the two zero vectors in each switching cycle. Each class has four sequencing schemes: rising-edge aligned, falling-edge aligned, symmetrical aligned, and alternative sequence. The examples of Class I sequencing schemes are shown in Figure 9-5 for two consecutive switching periods. The examples of Class II sequencing schemes are also shown in Figure 9-5 for two consecutive switching periods. All the examples assume that the reference vector locates in prism I tetrahedron 1, and phase A carries the largest current.



Class I sequencing schemes
 (a) rising-edge aligned; (b) falling-edge aligned;
 (c) symmetric aligned; (d) alternative sequence



Class II sequencing schemes
 (a) rising-edge aligned; (b) falling-edge aligned;
 (c) symmetric aligned; (d) alternative sequence

Figure 9-5. Sequencing Schemes.

9.2.3 3-D SVM scheme with zero vector disabled

Since the fluctuation of the neutral point voltage may cause the common-mode (CM) voltage, in order to mitigate the CM EMI, one of the ideas is to minimize the fluctuation of the neutral point. Thus the following SVM scheme can be employed.

The idea is that at any time, if there are two of these four legs connected to DC high while the other two are connected to the DC low, then the load neutral point voltage can be well balanced to half of the DC voltage, thus minimizing the voltage fluctuation.

Based on this idea, among the 16 voltage space vectors distributed in the 3-D coordinate, only six vectors can be utilized. They are as follows: pnpn, ppnn, npnp, nppn, nnpp, and pnpn. The spatial distributions and the projection on the $\alpha\beta$ plane are shown in Figure 9-6.

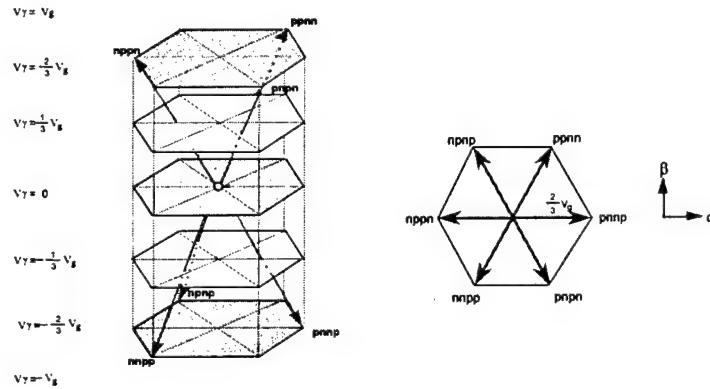


Figure 9-6. Balanced vectors without zero vectors.

Since the applicable vectors are reduced to six, the SVM realization also can be simplified. We no longer need to determine which tetrahedron the reference vector is located in. The selection of vectors can only base on the projection of the reference vector on the $\alpha\beta$ plane, which means among three dimensional components of the reference vector, only α and β information is needed to determine the vectors to be used. Similar to the 2D SVM, we easily can identify which sector in the $\alpha\beta$ plane the projection of the reference vector is in; then, we can always select the four vectors closed to the sector to synthesize it. For example, if we know the reference vector is located in prism I, i.e. sector I in the $\alpha\beta$ plane, then we can use the vectors $V_1 = [pnpn]$, $V_2 = [pnpn]$, $V_3 = [$

ppnp], $V_3 = [\text{ppnn}]$, and $V_4 = [\text{npnp}]$ to synthesize it. The duration of each applied switching vector can be calculated as

$$\begin{bmatrix} d_1 \\ d_2 \\ d_3 \\ d_4 \end{bmatrix} = \frac{1}{V_g} \begin{bmatrix} -\frac{1}{2} & -\frac{\sqrt{3}}{2} & \frac{1}{4} & \frac{1}{2} \\ 1 & 0 & -\frac{1}{2} & 0 \\ \frac{1}{2} & \frac{\sqrt{3}}{2} & \frac{1}{2} & 0 \\ -1 & 0 & -\frac{1}{4} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} \dots\dots\dots (3)$$

9.3 Over-modulation issue

9.3.1 Introduction

Voltage source inverters (VSIs) have been used widely in power electronics systems. Due to simple and effective digital implementation, the SVM technique is employed broadly and the over-modulation aspect of various SVM schemes has attracted many research activities.

For a utility application, since the load can be arbitrary (e.g. balanced and/or unbalanced, linear and/or nonlinear), a three-phase four-wire converter system is needed to provide the return neutral path. To utilize the DC bus voltage fully, a four-legged inverter configuration was proposed, and, accordingly, with the additional neutral leg, a 3-D SVM method was adopted for the control.

Compared with the traditional three-legged converter system with a 2-D SVM method, the four-legged converter along with 3-D SVM gives more flexibility under unbalanced load conditions, but gets more complex at the same time. However they still share similar features to the traditional three-legged converter, such as the over-modulation. There are currently many research efforts with 2-dimensional SVM schemes; however, for the 3-D SVM, little work has been carried out on over-modulation research.

Currently, for the three-legged inverter, since the application is mainly for motor drive, the over-modulation schemes focus on better utilizing DC voltage to improve the current regulator performance; the over-modulation boundary can be set as the hexagon. While

for utility applications, the main purpose is to provide a constant three-phase balanced pure sinusoidal voltage, this hexagon boundary may distort the output voltage waveform.

9.3.2 Over-modulation in SVM schemes

Over-modulation is a special mode in which the reference vector goes into the region where the vector is too large to be synthesized by the given vectors within one switching cycle. Suppose $V_{ref} = V_1 \cdot d_1 \cdot T + V_2 \cdot d_2 \cdot T + V_3 \cdot d_3 \cdot T + V_0 \cdot d_0 \cdot T$, when over-modulation occurs, $d_1 + d_2 + d_3 + d_0 > 1$. However, in physical implementation, for constant switching frequency, there always exists the constraint that $d_1 + d_2 + d_3 + d_0 = 1$, so V_{ref} cannot be synthesized by V_1, V_2, V_3 and V_0 within one switching period T . Without the over-modulation correction schemes, the actually synthesized reference vector, V'_{ref} , which is truncated switching cycle, is far away from the reference vector we want, V_{ref} . Using V'_{ref} instead of V_{ref} in the control would cause distortion in the output. For VSIs the output voltage waveform will be distorted from the reference waveform, and unwanted harmonics will be introduced by the over-modulation.

For VSI-feed motor drive applications, what we want first is the input sinusoidal current of the motor to get good performance. As long as the VSI output current can satisfy the control requirement, we can allow some distortion in the output voltage waveform. To get full utilization of the DC bus voltage, some of the over-modulation region often is used in the design with modified SVM algorithms. These algorithms are studied widely by many researchers now.

For the VSI in the utility application, since the output voltage waveform is the first consideration, the unwanted distortion is not allowable. The system should be kept from entering the over-modulation region.

9.3.2.1 Over-modulation in conventional 2-D SVM

With over-modulation, the magnitude of the fundamental output voltage can be higher at the price of a much larger distortion. It is useful to boost the output voltage, or for the transient when the reference vector is outside the hexagon. When the reference vector points outside the hexagon, the duration calculation results in meaningless negative duty

ratios. Since the achievable reference vector is within the hexagon, it is necessary to modify the reference vector within the boundary when the reference vector is outside the hexagon.

To synthesize a balanced three-phase sinusoidal output waveform in a 2-D α - β plane, the trajectory of the reference vector is a circle with the radius related to the modulation index. We can draw an inner circle tangential to the hexagon, shown as Figure 9-7 (a). The radius of this inner circle indicates the maximum modulation index for a non-over-modulation case. When the length of the reference vector is larger than the radius of this circle, over-modulation occurs. Whenever over-modulation occurs, there are two solutions: (1) to guarantee the output sinusoidal voltage waveform without distortion, the reference vector should be modified within this circle; (2) to utilize the DC bus voltage fully while output voltage distortion is allowable, set the hexagon as an over-modulation boundary, so that the trajectory of modified reference vector becomes the solid line as shown in Figure 9-7 (b).

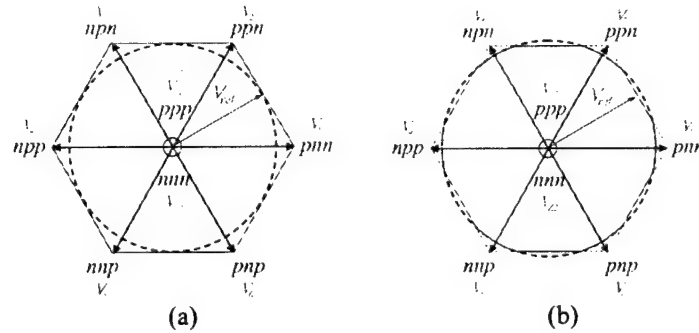


Figure 9-7. Over-modulation boundary in α - β plane.

9.3.2.2 Over-modulation in 3-D SVM

The over-modulation boundary decided by physical implementation for the 3-D SVM is similar to that for the 2-D version. From equation (2), if we limit d_1 , d_2 , d_3 and d_0 to be less than 1, then use the space analysis geometry method, with the vectors we can describe the boundary equation, which in the graphic mode would become exactly the four surface planes of the tetrahedron. For example, in tetrahedron 1 of prism I, the boundary surface is the four planes decided by the points (pppp, pnnn and pnpn), (pppp, pnnnn and ppnp), (pppp, pnpn and pnnp), and (ppnp, pnnn and pnpn), respectively. Since

the former three boundary planes are satisfied naturally by the vectors (thus the tetrahedron) selection in SVM, we only should care for the boundary plane decided by the three points (ppnp, pnnn and pnpn) in the implementation. This plane is exactly the result of constraint $d_0=0$ (or $d_1+d_2+d_3=1$). Similar results can be applied to the other tetrahedrons. Thus in prism I, the over-modulation boundary surface can be shown as planes I, II and III in Figure 9-8. So, instead of the hexagon in the 2-D case, the over-modulation boundary surface is shown as Figure 9-9, and there are three over-modulation surfaces in each prism. The over-modulation surfaces confine the attainable region. When the reference vector intersects with any of the three over-modulation surfaces, the reference vector should be modified within the over-modulation surface.

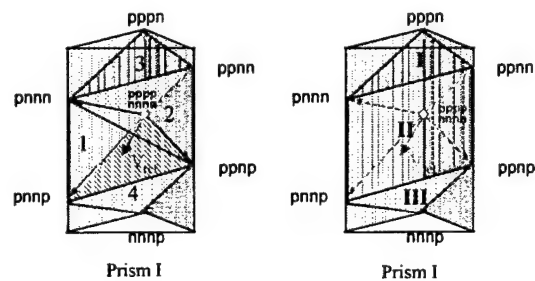


Figure 9-8. Over-modulation boundary surfaces in prism I.

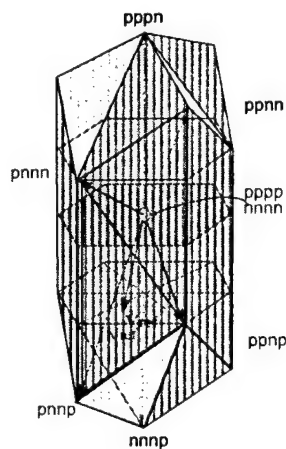


Figure 9-9. Over-modulation boundary surfaces.

Over-modulation happens in the following situations: (1) large transient; (2) highly unbalanced load; (3) highly nonlinear load; (4) fault mode operation. When the reference vector is outside the region confined by the surfaces given by the 24 tetrahedrons, the 3-D SVM goes into over-modulation mode. The duty ratios of switching vectors may become

negative if the reference vector is not modified. Thus, in actual implementation, since the reference vector cannot be synthesized by the given vector in the given switching cycle, the output waveform will be distorted greatly, as can be seen from both experimental and simulation results shown in Figure 9-10 and Figure 9-11, respectively.

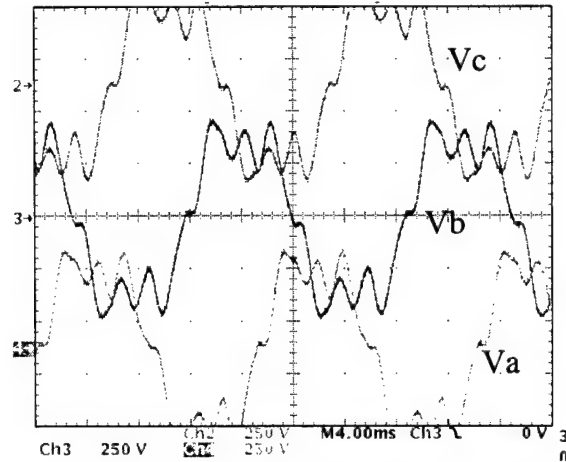


Figure 9-10. Experiment output voltage waveform when over-modulation occurs.

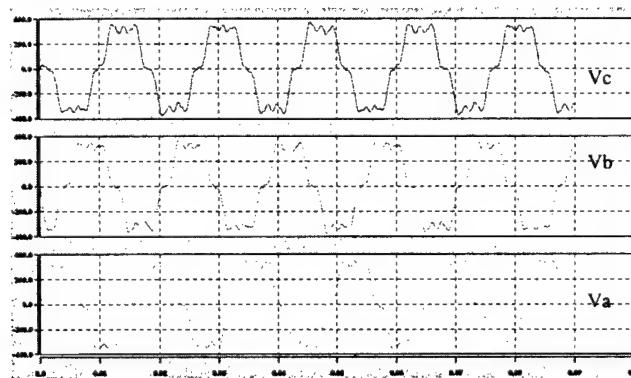


Figure 9-11. Simulated output voltage waveform when over-modulation occurs.

9.3.3 3-D SVM over-modulation correction method

In 3-D SVM, there are two correction schemes to deal with the reference vector entering into the over-modulation region case. One scheme is constrained by physical implementation, the boundary of which is discussed in the above Section III. When an over-modulation case happens, the reference vector is modified to point to the boundary surface; that is, the length of the reference vector will shrink to hit the boundary surface while the direction remains the same. For convenience, we name this method Scheme 1. The reference vector is limited on a cylindrical boundary.

The other scheme is constrained by no distortion on the output voltage waveform; similar to the 2-D SVM case, this constraint is stricter than the former one. Actually, the 3-D SVM is the super set of the 2-D SVM in a small γ axis component sense. That is, if the reference vector is located in tetrahedrons 1 or 2 in each prism, then the projection of the reference vector trajectory on the α - β plane should be the same as the 2-D SVM case. Therefore, we can extend the method used in the 2-D SVM to this case.

Considering the γ axis, the inner circle boundary in the 2-D SVM case becomes a cylinder in the 3-D SVM case. The projection of the cylinder and the boundary set by Scheme 1 in tetrahedrons 1 and 2 in each prism in the α - β plane would be exactly the same as the 2-D SVM case. However, when the reference vector resides in tetrahedrons 3 or 4 in each prism, since the projection of the boundary set by the scheme is no longer the hexagon on the α - β plane, we cannot use the cylinder as the over-modulation boundary. Instead, we can use the sphere which is tangent to those boundary planes set by the scheme in tetrahedrons 3 and 4 in each prism as the over-modulation boundary. When the reference vector is outside the sphere in tetrahedron 3 or 4, it should be shrunk to the sphere surface in the same direction. For convenience, we call this method Scheme 2, shown as Figure 9-12.

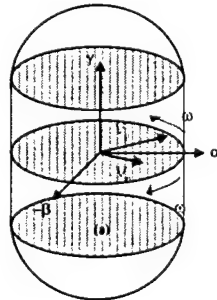


Figure 9-12. Over-modulation correction scheme 2.

9.3.4 Simulation results

For the inverter applied to the utility interface, Scheme 2 is more desirable as can be seen from the comparison of the following simulation results.

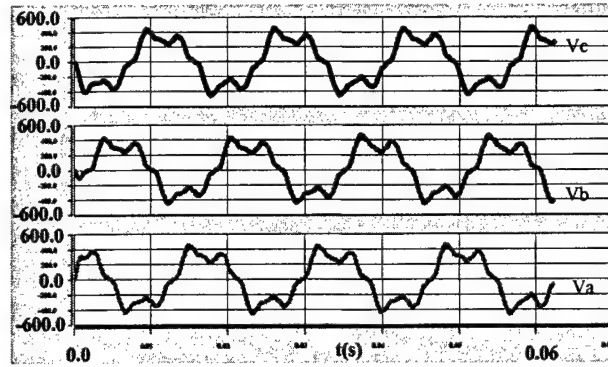
As we mentioned in section III (B), over-modulation could happen under fault mode and unbalanced load case. Here we just use two simulation cases to illustrate the improvement achieved by the two correction schemes:

- (1) Simulation of balanced load case (with 1.53Ω resistor in each phase) based on voltage open-loop control. The reference vector is set to beyond the surfaces shown in Figure 9-9, which mimics the controller fault mode happening.
- (2) Simulation of unbalanced load case (Phase A open, 1.53Ω resistor in each of the other two phases) based on the voltage closed-loop control on a 480-V, 150-kW four-legged inverter system. Both of the simulation cases use 800-V DC link voltage.

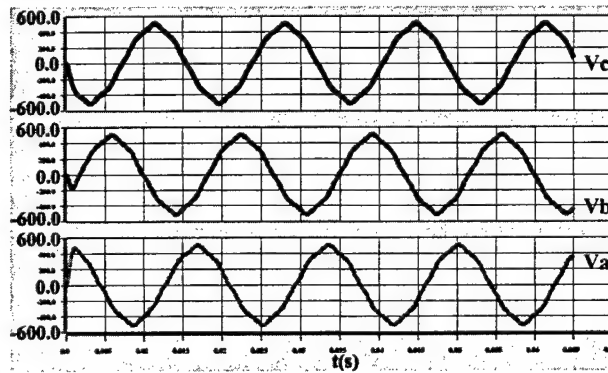
Figure 9-13(a) shows the simulated voltage waveforms of the balanced load without over-modulation correction schemes. The waveforms are distorted, but three phase voltages are still balanced. However, with Scheme 1, the waveforms can be improved to be close to sinusoidal, which can be seen from Figure 9-13(b). While Figure 9-13(c) illustrates that with Scheme 2, the output waveform can be improved even more.

This effect can be seen more clearly from the simulated voltage waveforms of the unbalanced load case, which are shown in Figure 9-13(d), Figure 9-13(e) and Figure 9-13(f), respectively. Without the over-modulation correction schemes, the output voltage waveforms are distorted with significant high frequency harmonics oscillation, shown in Figure 9-13(d). With Scheme 1 the voltage distortion remains in the unbalanced case [Figure 9-13(e)]. However, with Scheme 2, the distortion can be eliminated mostly, as shown in Figure 9-13(f).

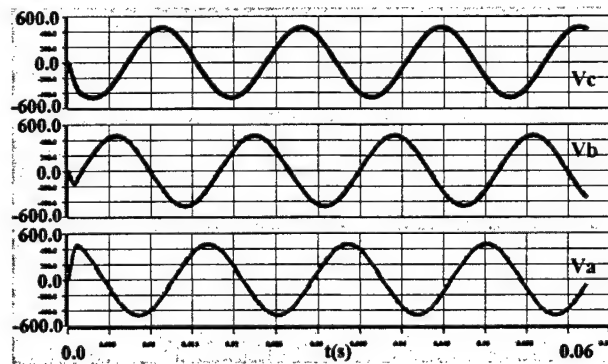
The improvement of the total harmonic distortion (THD) by different over-modulation correction schemes can be seen from the frequency analysis results of the phase voltages, as shown in Table 9.1. Using Scheme 2, the output voltage THD is reduced by more than ten times in both balanced and unbalanced load case.



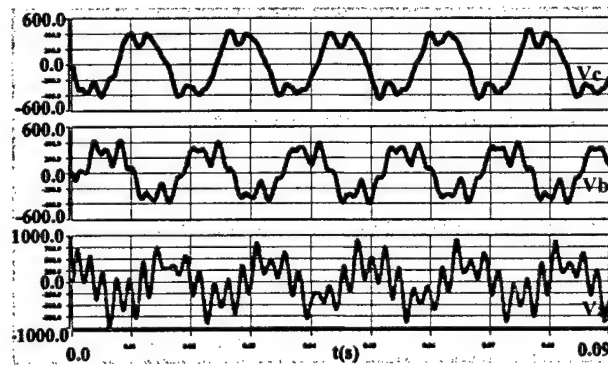
(a) Balanced load case, without over-modulation correction scheme



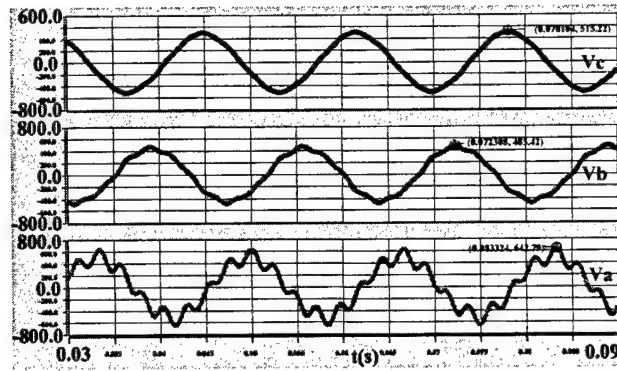
(b) Balanced load case, with over-modulation correction Scheme 1



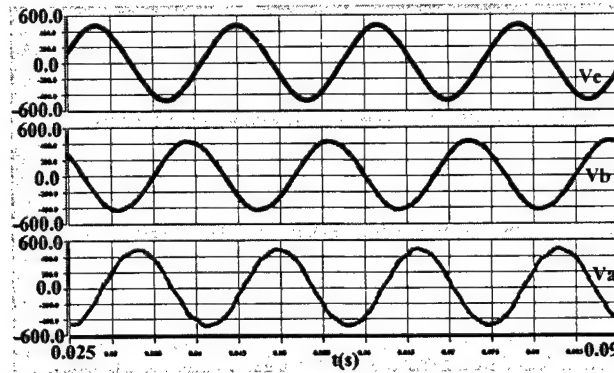
(c) Balanced load case, with over-modulation correction Scheme 2



(d) Unbalanced load case, without over-modulation correction scheme



(e) Unbalanced load case, with over-modulation correction Scheme 1



(f) Unbalanced load case, with over-modulation correction Scheme 2

Figure 9-13. Simulated output voltage waveform in over-modulation modes.

Table 9.1 THD COMPARISON OF OUTPUT VOLTAGE WAVEFORMS

	(a)	(b)	(c)
V_a	32.17	3.797	1.149
V_b	34.32	3.725	1.089
V_c	32.97	3.757	1.2
	(d)	(e)	(f)
V_a	67.66	22.34	3.003
V_b	38.84	5.877	1.604
V_c	27.84	2.934	2.408

The waveforms and THD analysis results show that in both balanced and unbalanced load case, the output voltage waveforms can be improved significantly with the proposed over-modulation correction schemes. However, in unbalanced load case, Scheme 1 cannot give satisfactory results in all of the three phase output voltage waveforms. With

Scheme 2, only little distortion is observed in the output voltage waveforms, and the THD for all three phase output voltages can be suppressed to below 3.1%.

However, the penalty for Scheme 2 is the output voltage reduction. From the Table 9.2 we can see that compared with Scheme 1, there is nearly 6% voltage RMS value decrease with Scheme 2.

Table 9.2 COMPARISON OF OUTPUT VOLTAGE RMS VALUES (UNIT V)

	With Scheme 1	With Scheme 2
Theoretical Value	342	326
Phase A	339	320
Phase B	339	318
Phase C	339	318

9.3.5 Summary

For utility interface application, the converter output voltage distortion is undesirable. According to both simulation and experimental results, the voltage distortion can be caused by over-modulation operation. Therefore, the over-modulation operation should be limited or corrected.

Using analogy, in this section the 3-D SVM can be considered as an extension of the 2-D SVM used in conventional three-legged converters. However, the over-modulation of the 3-D space vector is much more complicated than that of the 2-D SVM space vector. This section then defined the 3-D SVM over-modulation boundary as a hexahedron with the space geometrical analysis. Two over-modulation correction schemes are proposed to confine the SVM operation within the hexahedron.

The proposed over-modulation schemes along with the system without over-modulation correction are compared with time-domain simulation and harmonic frequency analysis. With the proposed Scheme 1, the output voltage waveform quality can be improved, but distortion can be severe under unbalanced load condition. With the proposed Scheme 2, which confines the voltage vector to an inner surface, the voltage distortion can be nearly eliminated. However, its available magnitude is reduced.

9.4 Common mode components comparison for different SVM schemes

9.4.1 Introduction

A large number of pulse width modulation (PWM) schemes for three phase inverters have been studied in the last two decades. To evaluate different modulation strategies, one criterion is the total harmonic distortion (THD) of inverter output voltage, which can be calculated from the output differential voltages and their spectrum. Recently some attention has been paid to the common mode voltage generated by the inverter and to the impact that the inverter modulation techniques have on common mode conducted emissions.

For utility applications, a three-phase four-wire converter is preferred because the return neutral path can deal with the arbitrary load: balanced and/or unbalanced, linear and/or nonlinear. To utilize the DC bus voltage fully, a four-legged inverter configuration can be adopted. Accordingly, with the additional neutral leg, different 3-D SVM methods were proposed and compared in various aspects such as THD and switching loss. However, there are few papers discussing the common mode EMI issue for different 3-D SVM schemes.

In this section, the relationship between switching and common mode voltage will be introduced first; then the simulations will be performed for different 3-D SVM schemes based on the SABER switch model. After that, the results from different SVM schemes will be compared and discussed.

9.4.2 Switching and common mode voltage

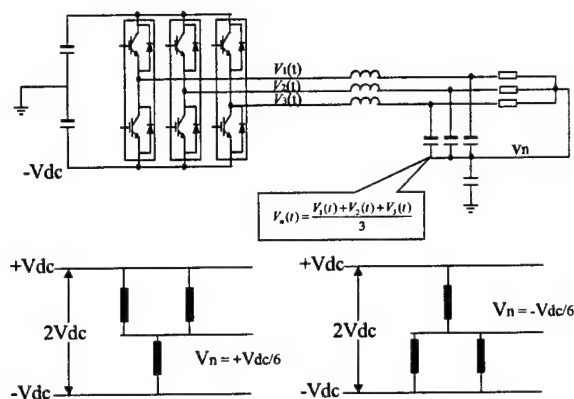


Figure 9-14. Neutral point voltage fluctuation in 3-phase inverter.

In three-legged three-phase inverters, different switching combinations can determine different neutral point voltages, as illustrated in Figure 9-14. The fluctuation of the neutral point voltage produces the common mode voltage. Because of the existence of the loop created by the parasitic capacitive coupling between the load and ground, the common mode current can flow through the earth ground and back to the source; thus, the common mode voltage and current can cause EMI problems. The same phenomenon exists in four-legged inverters.

9.4.3 Simulation of different SVM schemes on common mode components

As shown above, the common mode voltage is related to the switching combinations; thus, different SVM schemes may affect the common mode EMI results, which can be seen from the following simulations. The circuit illustrated in Figure 9-15 is used to perform the simulation, and the simulation is based on open-loop control with output voltage to be 277 Vrms, and 800V DC bus voltage. Here we assume in the neutral-ground coupling channel, the parasitic capacitor is 60 pF, the leakage resistor is 100Meg Ω , and the switching frequency is set to 5 kHz. The waveforms of neutral point (n) voltage and neutral to ground current are captured and their spectrum analyses are performed. Among these waveforms, the upper one is neutral to ground current, and the lower one is the neutral point voltage.

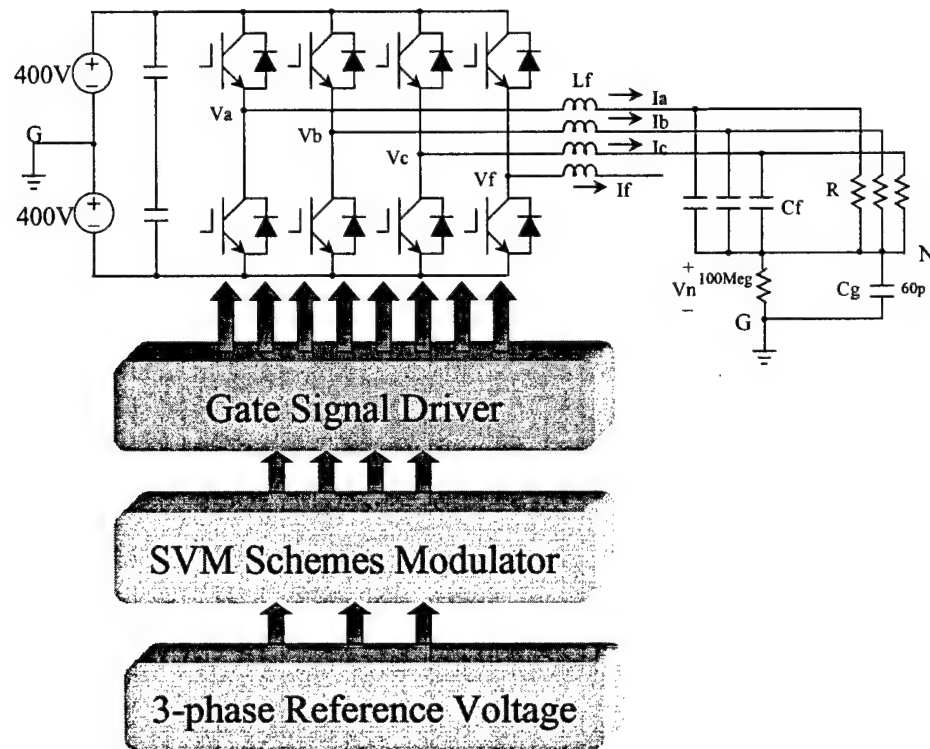
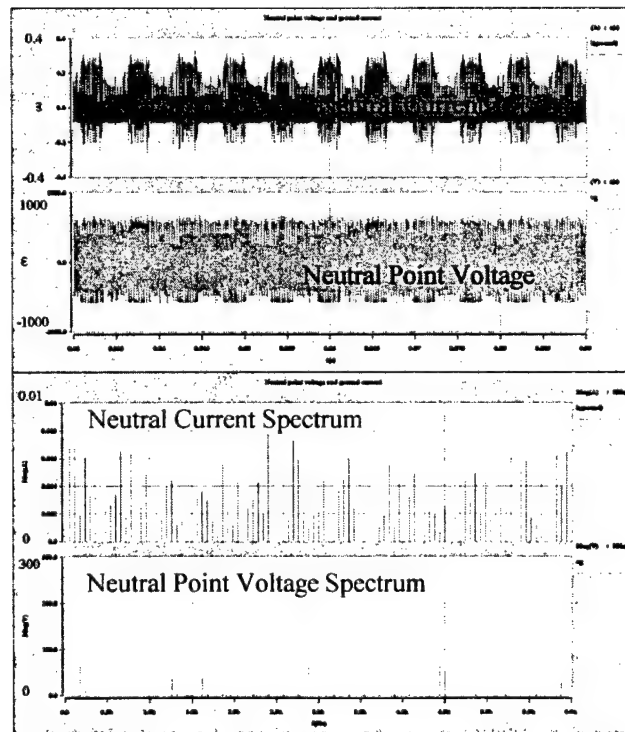
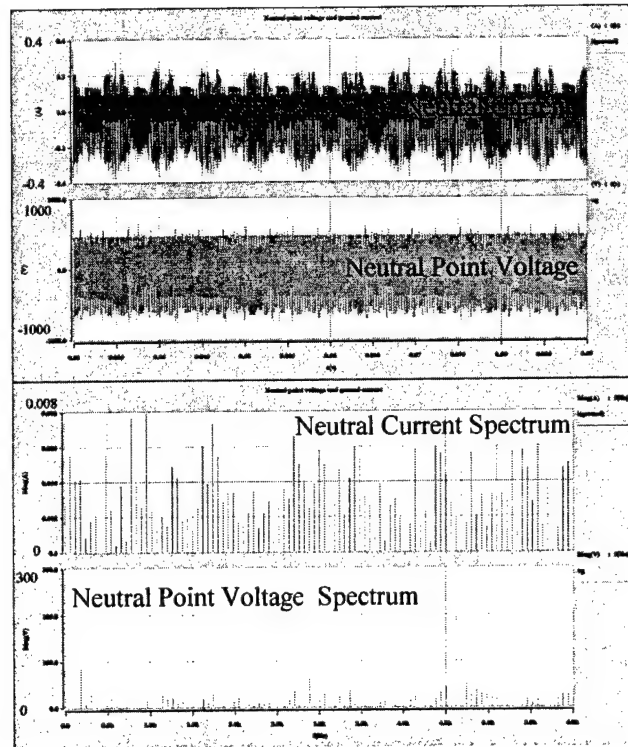


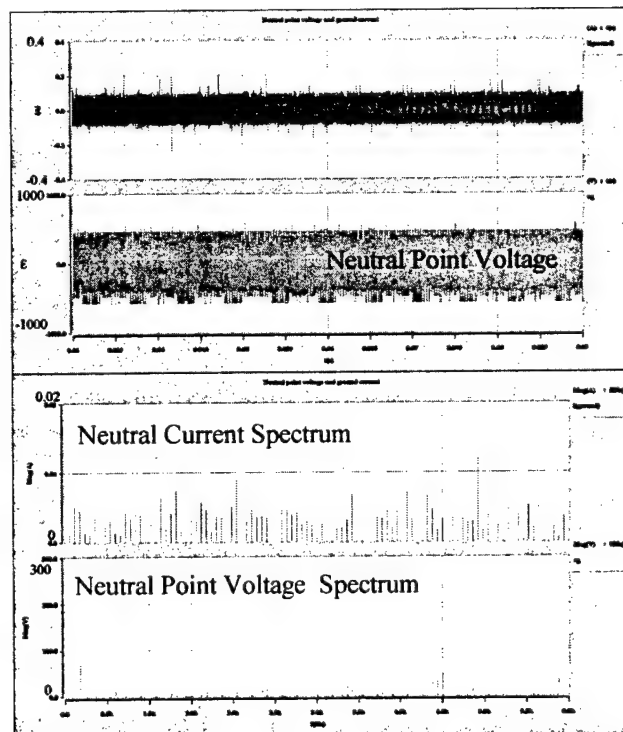
Figure 9-15. Simulation circuit.



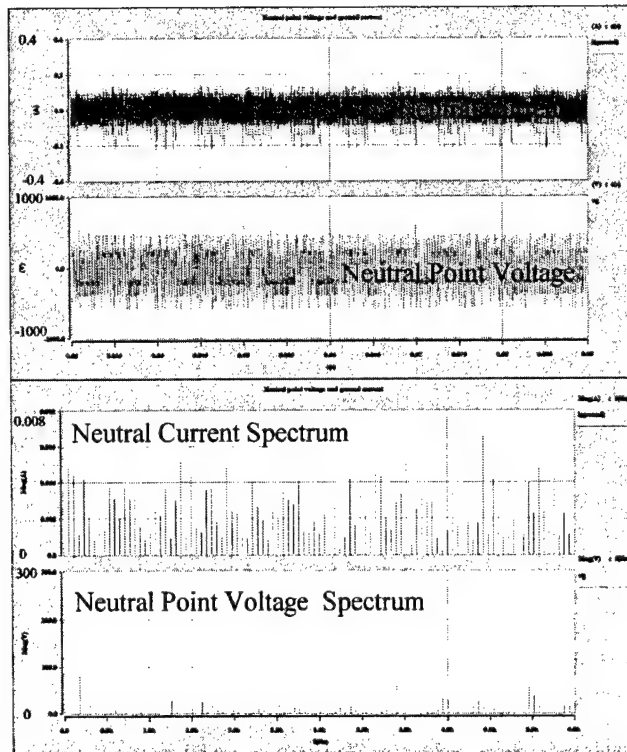
SVM1



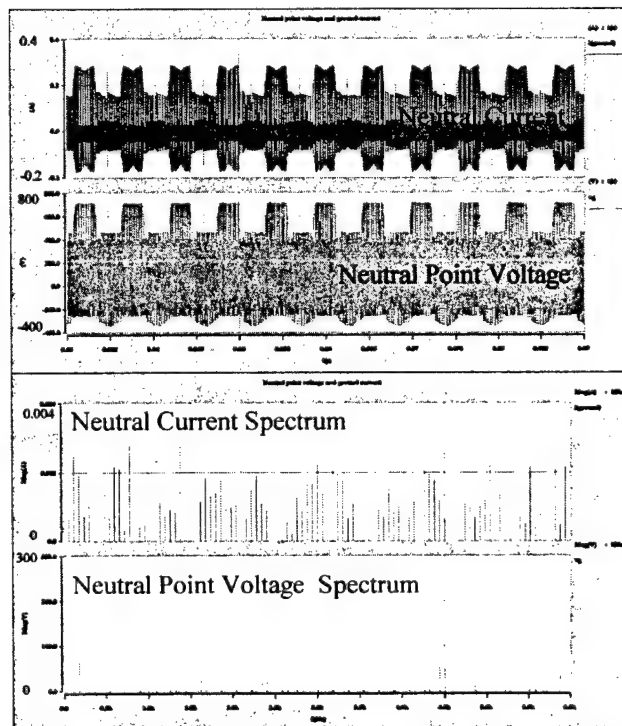
SVM2



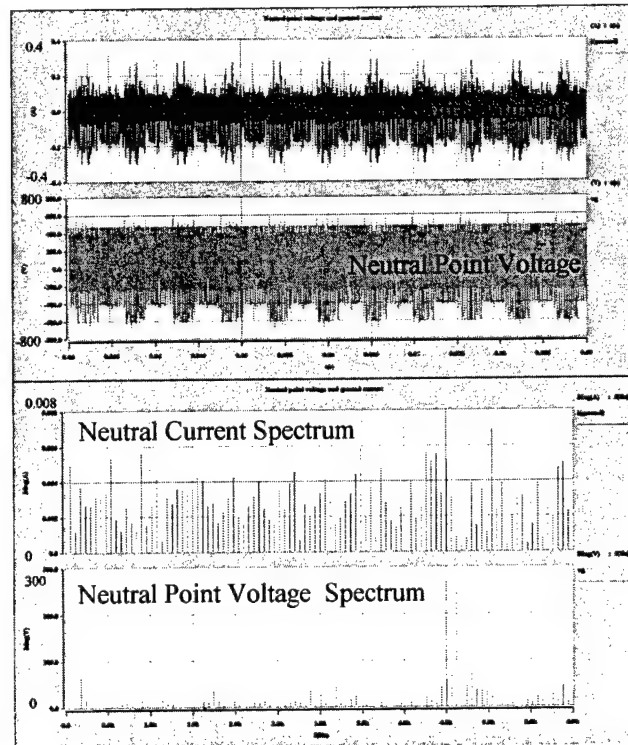
SVM3



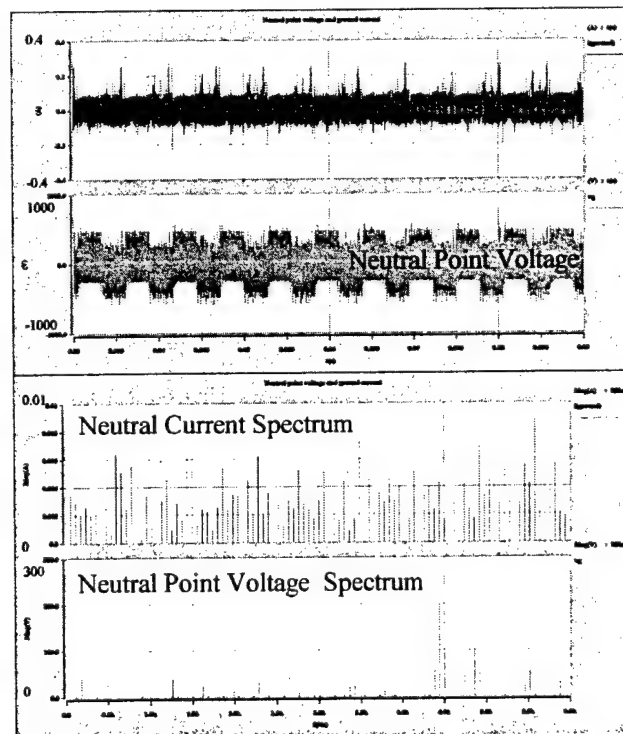
SVM4



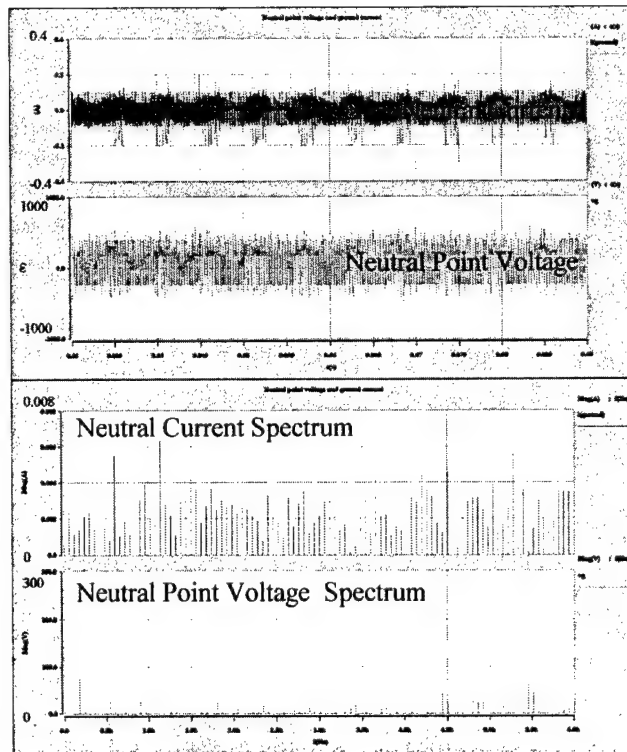
SVM5



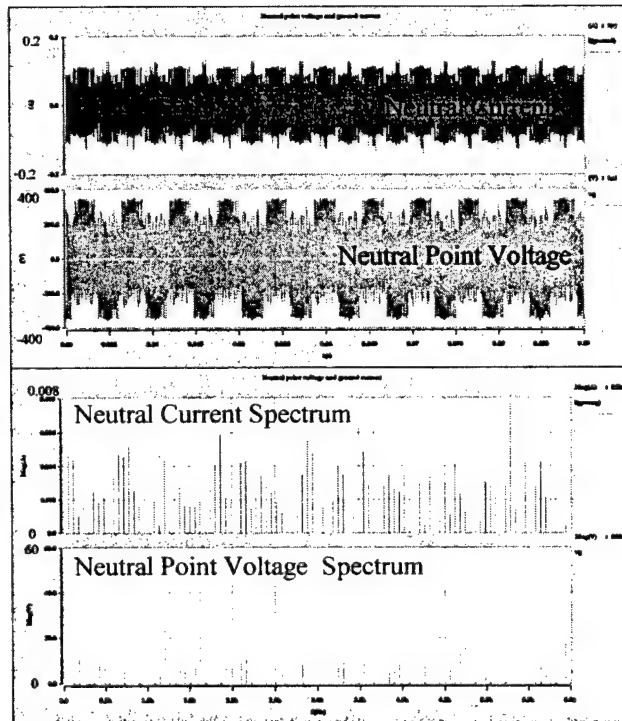
SVM6



SVM7



SVM8



SVM9(w/o zero vectors)

Figure 9-16. Simulation results.

From the simulation results shown in Figure 9-16, we can see, among the eight different sequencing schemes with zero vectors, that there are slight differences between the waveforms. The neutral point voltage magnitudes of Class II schemes are a little smaller than those of the corresponding schemes in Class I. This makes the neutral current magnitudes smaller as well. This is caused by the fewer switching combination changes within one switching cycle in Class II schemes. From the neutral current waveforms, we can also find that the symmetric schemes have the smaller magnitudes in the same class. There is no significant difference between the spectrum distribution of the neutral point voltage; however, from the spectrum distribution of the neutral currents, we can see that energy is always concentrated around the switching frequency (5 kHz in the simulations).

While, for the balanced SVM scheme without using zero vectors (SVM9), the magnitudes of both neutral point voltage and neutral current are small, from the spectrum of the neutral voltage we can find that the energy is spread to the whole frequency scale. The maximum magnitude is reduced greatly.

9.4.4 Selection of SVM schemes

For Class I schemes, there are eight switching actions in each switching period for the rising-edge aligned scheme, the falling-edge aligned scheme, and the symmetrical aligned scheme. Although the alternative aligned has six switching actions in each switching period, and thus reduces its switching losses, it suffers from a large harmonic content at half of the switching frequency since the switching pattern repeats every two switching periods. The rising-edge and falling-edge aligned schemes have larger harmonic contents and yield larger distortion than the symmetrically aligned schemes. Due to its symmetry, the symmetrically aligned Class I scheme gives the least harmonic distortion. Aside from the above harmonic performance, the symmetric schemes also give better EMI performance on neutral current.

By selectively using the two zero vectors in Class II schemes, the phase carrying the highest current is not activated. Compared with Class I schemes, they save two switching actions for the highest current phase for rising-edge aligned, falling-edge aligned and symmetrical aligned schemes and save one switching action for the alternative aligned.

Thus the switching loss can be reduced and the CM EMI performance can be improved with Class II schemes.

Considering the CM EMI aspect, the balanced scheme that does not use zero vectors shows best performance from the voltage spectrum. However, this scheme suffers from large inductor current ripples. It also has smaller voltage regulate headroom, the non-over-modulation region is much smaller. To get the same output voltage, it needs higher DC voltage compared with the other schemes using all 16 space vectors.

Overall, the symmetrically aligned Class II scheme is a good compromise between the switching losses and the harmonic contents, as well as a favorable CM EMI aspect.

9.4.5 Summary

In this section, common mode EMI issues in 3-D SVM schemes brought up and discussed. Nine 3-D SVM schemes were investigated from an EMI point of view. The SVM scheme selection is discussed. Of the nine schemes, the symmetrically aligned Class II scheme (SVM2) is the best selection.

9.5 Sub-system control design and test

9.5.1 System control block diagram

The four-leg inverter system can be modeled in DQO coordinates by switching averaging technology as:

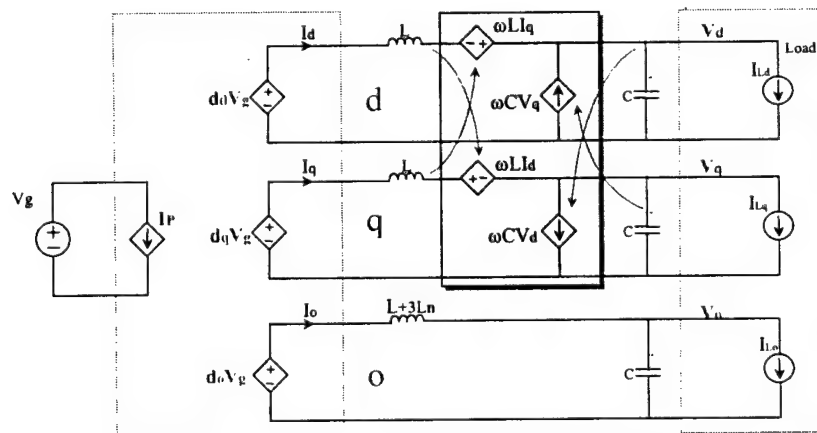


Figure 9-17. Average model of the main inverter in DQO coordinates.

In the implementation, this 4-leg inverter system is controlled by the SHARC DSP based digital controller. The whole controlled system is shown in Figure 9-18.

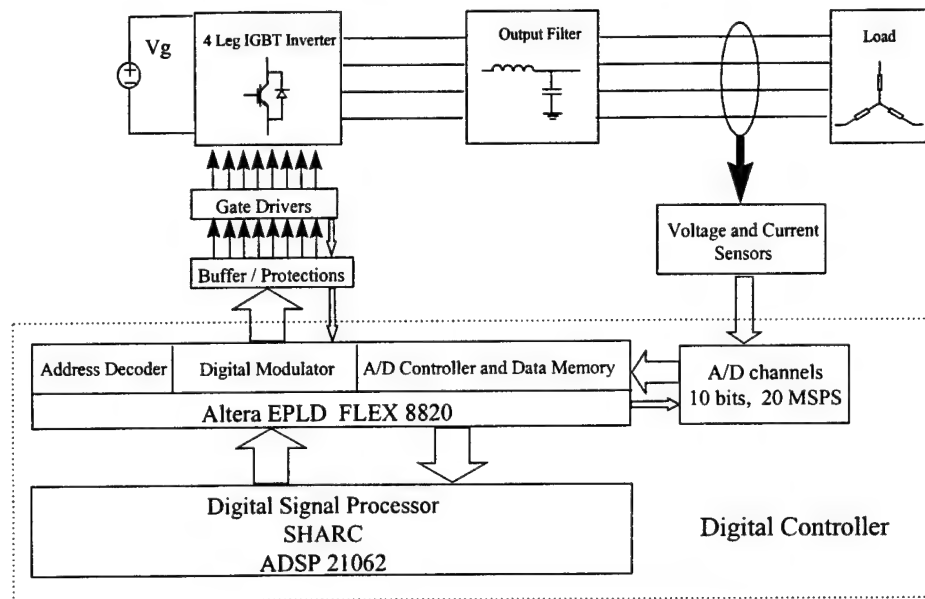


Figure 9-18. DSP controlled system block diagram.

Since the ultimate goal is to control the output voltage, a voltage loop feedback control is most straightforward. In terms of control loop design, assuming the DC link voltage is an ideal voltage source, the system control block diagram with voltage loop compensators is shown in Figure 9-19. For the sake of simplicity, the small signal labels '^' are dropped.

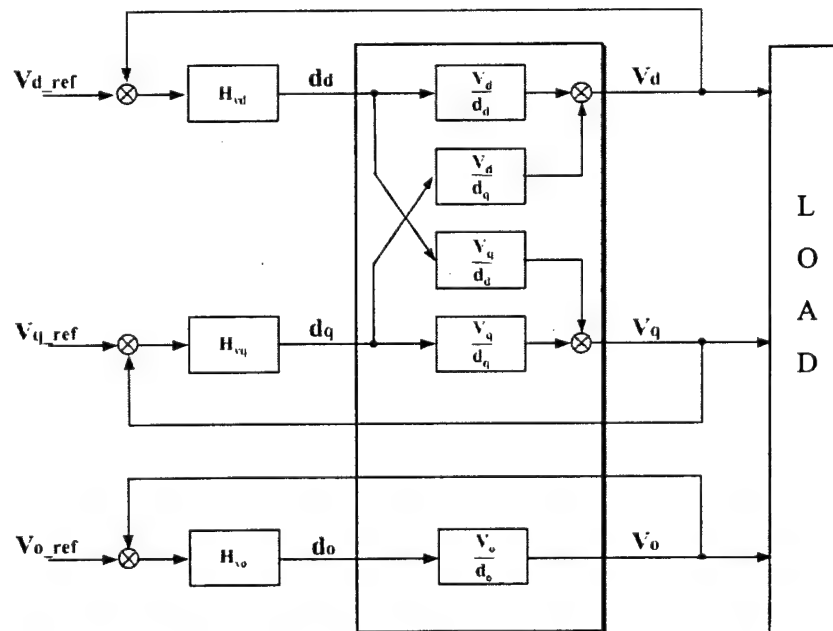


Figure 9-19. System control block diagram with voltage loop compensators.

The small signal model of the power stage is represented by the transfer function blocks in the shaded boxes. The voltage loop includes three independent PI compensators H_{vd} , H_{vq} and H_{vo} for d, q and o channels to eliminate steady state error. Underminated load (i.e. three-phase load represented by three DC current sources to give the rated output power level) is used to guarantee the stability under no load condition. To emulate the power losses, 153 Ohm resistors, which are equivalent to 1% of the total power level, are used for each channel. Including a 350 μ s time delay caused by the digital sampling effect and the time delay due to the 3-D SVM with the symmetric sequencing scheme, the power stage control-to-output voltage transfer functions are plotted in Figure 9-20 at 150 kW power level. It can be seen that there are four poles and two zeros around the resonant

frequency (505 Hz) for the d and q direct transfer functions $\frac{V_d}{d_d}$ and $\frac{V_q}{d_q}$. Since the poles

and zeros are very close to each other, they almost cancel each other. Therefore, the transfer functions are similar to a second-order system, except for the complicated shape

around the resonant frequency. The o channel is a typical second-order system. $\frac{V_o}{d_o}$ has a

double pole at the o channel resonant frequency (320 Hz). It should be noted that the resonant frequency of the o channel is different from that of d and q channels, due to the presence of the neutral inductor. The larger the neutral inductor is, the lower the resonant frequency of the o channel is. Although the neutral inductor helps to reduce the current ripple, it is not desirable to have a low resonant frequency for the o channel from a control point of view. Therefore, there is a trade-off in the design of the neutral inductor.

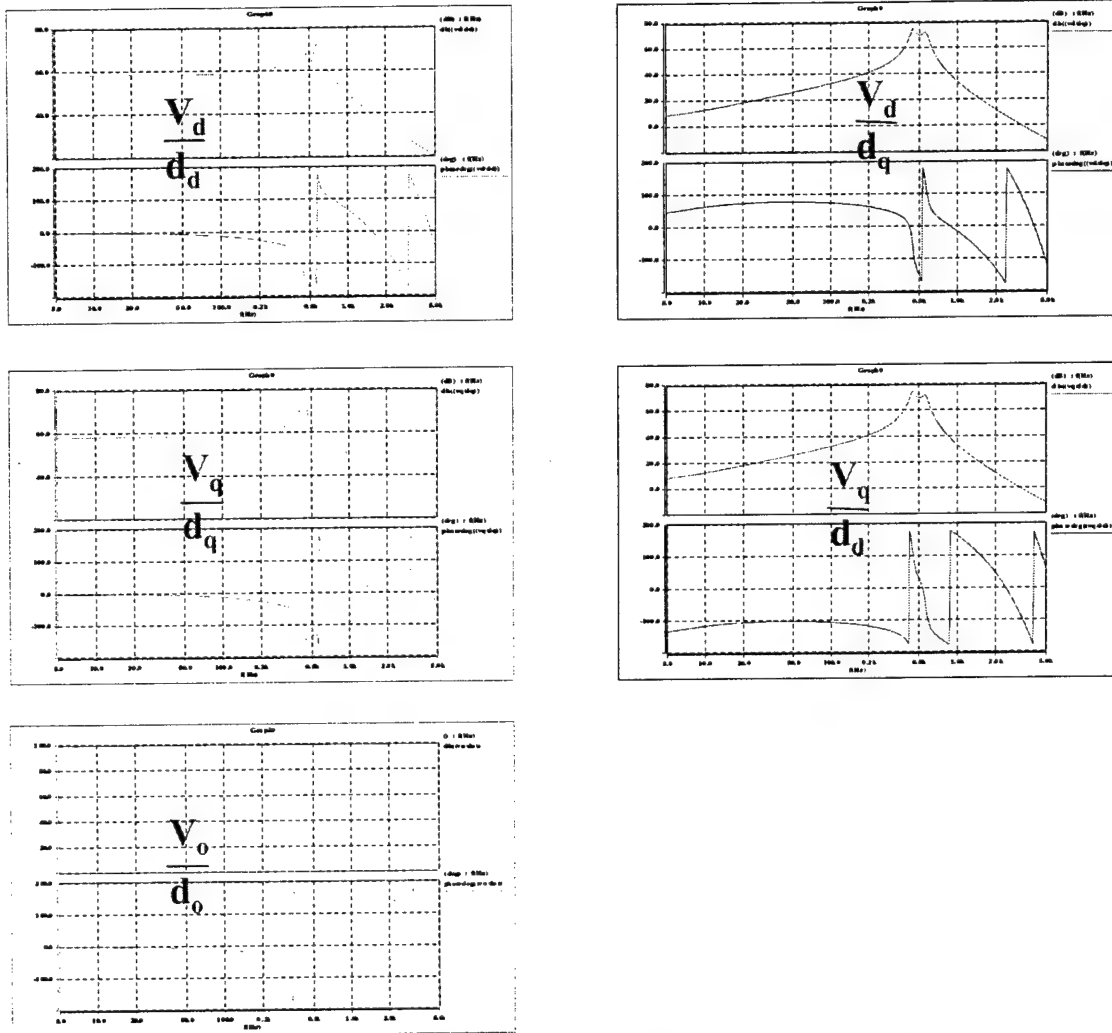


Figure 9-20. Control-to-output voltage transfer functions of a four-legged inverter with unterminated load at 150 kW.

(153 Ohm resistors are terminated at each channel to emulate the power losses, a time delay of 375 us is used to account for digital sampling delay and PWM delay)

The design of the PI compensators can be easily done by following the traditional design approach, putting a zero at the resonant frequency and adjusting the gain to have the desired cross-over frequency and gain and phase margins. However, special attention should be paid to the following three points.

First, it can be seen that the peaking of the control-to-output-voltage transfer function around the resonant frequency is more than 20 dB and the phase rolls down sharply to -180 degrees around the resonant frequency. Therefore, the cross-over frequency should be placed below one-tenth of the resonant frequency to avoid instability at a light load.

Second, there is a control ambiguity around the resonant frequency of the d and q channels due to the coupling transfer functions. It can be seen from the simulated transfer functions at the rated power level and the measured transfer functions at no load, as shown in Figure 9-21, that the coupling transfer functions $\frac{V_d}{d_q}$ and $\frac{V_q}{d_d}$ has an even higher gain than the direct transfer functions $\frac{V_d}{d_d}$ and $\frac{V_q}{d_q}$.

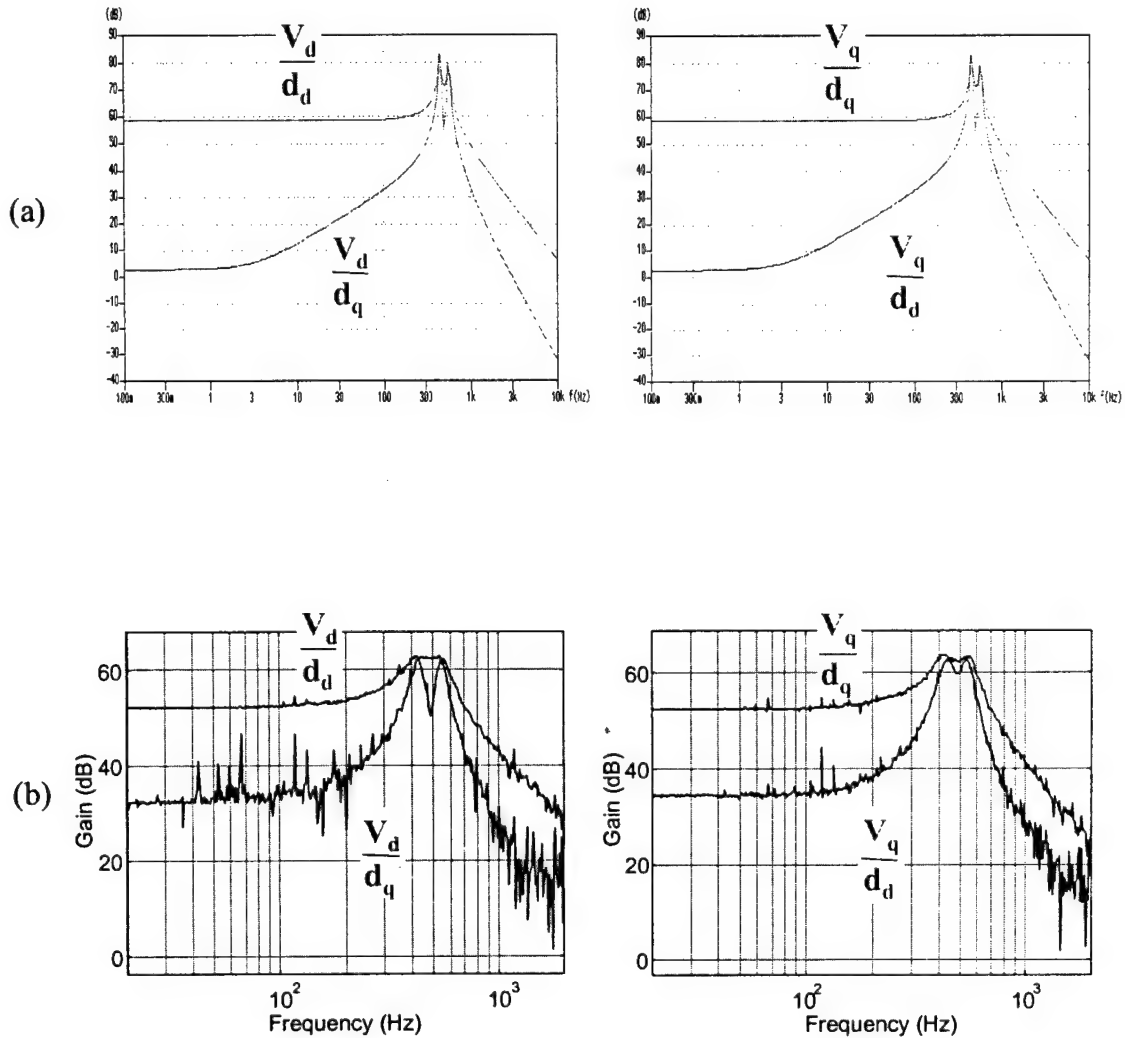


Figure 9-21. Control ambiguity around the resonant frequency at light load.

- (a) simulated direct and coupling transfer functions at 150 kW with unterminated load;
(b) measured direct and coupling transfer functions at no load.

Third, the impact of the load power factor on the control loop should be considered. Given the prototype load power factor range $[-0.8, 0.8]$, the control-to-output voltage

transfer functions are plotted in Figure 9-22 with the resistive load, capacitive load and inductive load. It can be seen that both the capacitive and inductive loads shift the resonant frequency. The capacitive load yields a lower resonant frequency. The zero of the originally designed PI compensator based on a resistive or unterminated load may not give enough phase margin with the capacitive load. Although the inductive load shifts the resonant frequency to a higher frequency, it leads to a higher peaking and phase drop due to an increased system order. Therefore, both the capacitive and inductive loads may give a worse case than a resistive or unterminated load.

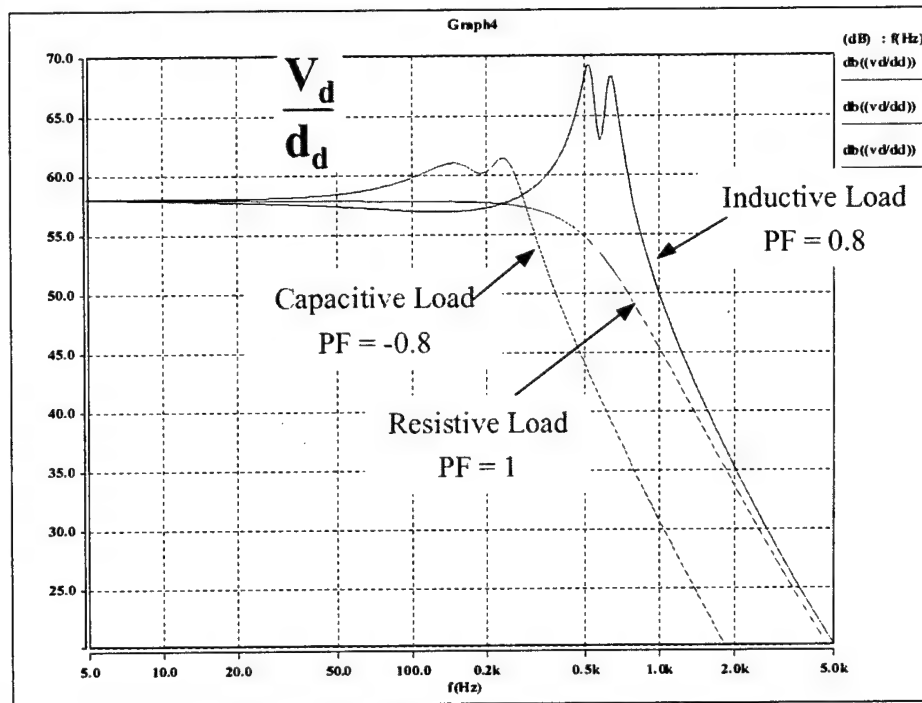


Figure 9-22. Impact of load power factor on control-to-output voltage transfer function – d channel V_d/D_d plot.

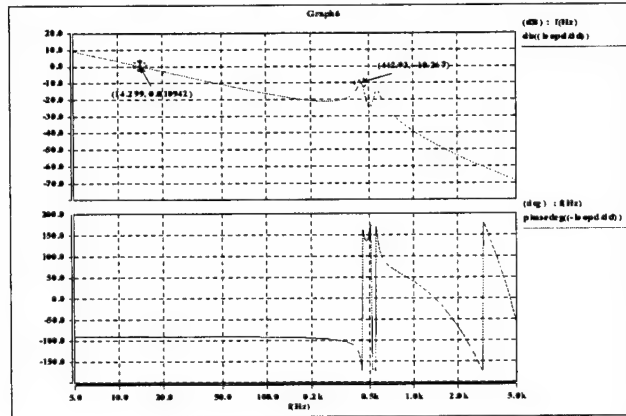
(output power level: 150 kW(kVA); Resistive load: 1.53 Ohm each phase; capacitive load: 780 μ F capacitor and 1.73 Ohm resistor and in parallel per phase; inductive load: 2.1 mH inductor and 1.316 Ohm resistor in series per phase)

When designing the PI voltage loop compensators, a 10 dB gain margin is set to ensure the stability under light load, capacitive and inductive load conditions. Therefore, the cross-over frequencies have to be designed to be less than 15 Hz for the d and q channels, and less than 6 Hz for the o channel, as shown in the voltage loop gain transfer function plots in Figure 9-23. The parameters of the voltage loop compensators that are finally designed are given in Table 9.3.

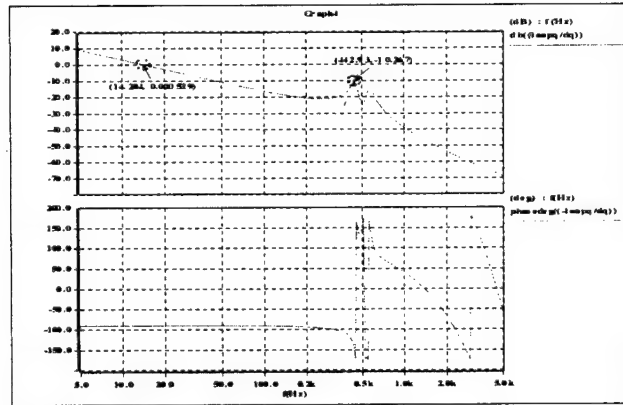
Table 9.3 Parameters of the Designed Voltage Loop Compensators

	K_p	K_i	Cross-Over	Phase Margin	Gain Margin
H_{vd}	$3.54e-5$	0.1107	15 Hz	90 degree	10 dB
H_{vq}	$3.54e-5$	0.1107	15 Hz	90 degree	10 dB
H_{vo}	$1.992e-5$	$4.117e-2$	6 Hz	90 degree	10 dB

(a) d channel



(b) q channel



(c) o channel

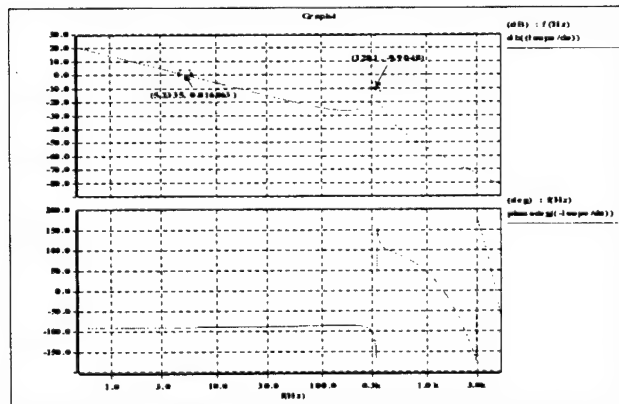


Figure 9-23. Voltage loop gain transfer functions of the four-legged inverter with PI compensators.

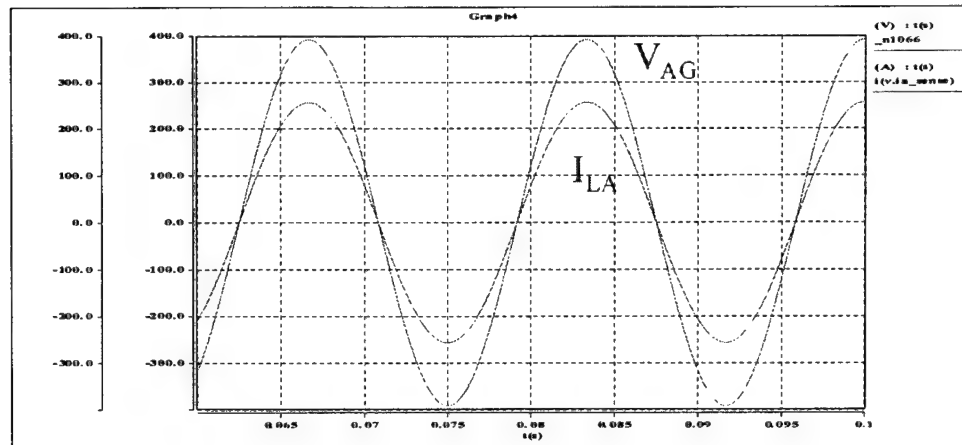
The low cross-over frequency would cause an unbalanced and distorted output voltage under unbalanced and/or nonlinear loads because there is almost no output impedance reduction with the closed voltage loop beyond the cross-over frequency.

9.5.2 *Simulation results*

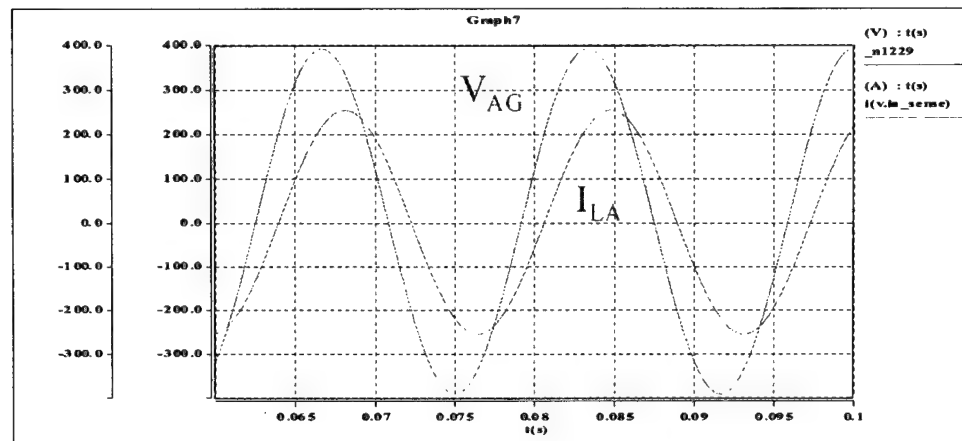
9.5.2.1 Balanced Load

Figure 9-24 shows the simulated Phase A output voltages and Phase A load currents with balanced resistive, capacitive and inductive loads at the rated output voltage and power level.

(a)



(b)



(c)

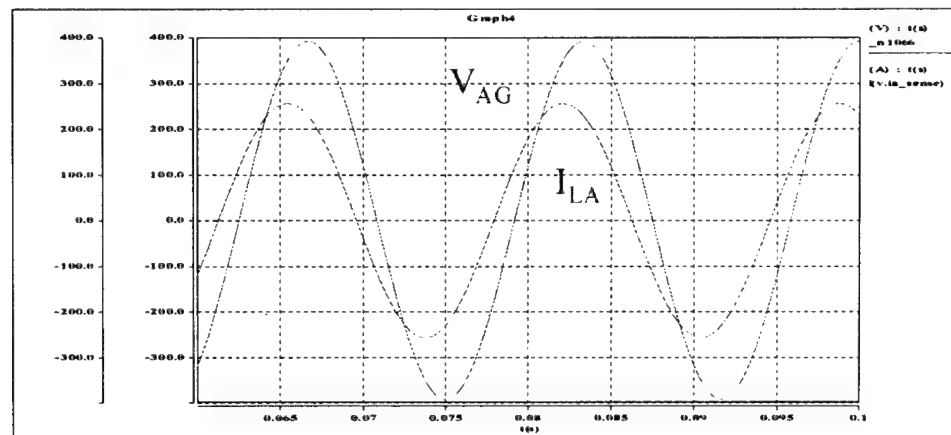


Figure 9-24. Simulation results with balanced linear load with different power factor at 150 kW (kVA) output power level.

(a) resistive load; (b) capacitive load; (c) inductive load

9.5.2.2 Nonlinear Load

A combination of balanced linear load and a three-phase diode bridge rectifier is used as the nonlinear load, as shown in Figure 9-25. The experimental waveforms of the Phase A output voltage V_{AG} and the Phase A load current I_{LA} are shown in Figure 9-30. The nonlinear load current THD is 12%. The resulting output voltage THD is 10.3%, which is much higher than the specification. Therefore, the designed control loops cannot give a satisfactory performance for nonlinear loads.

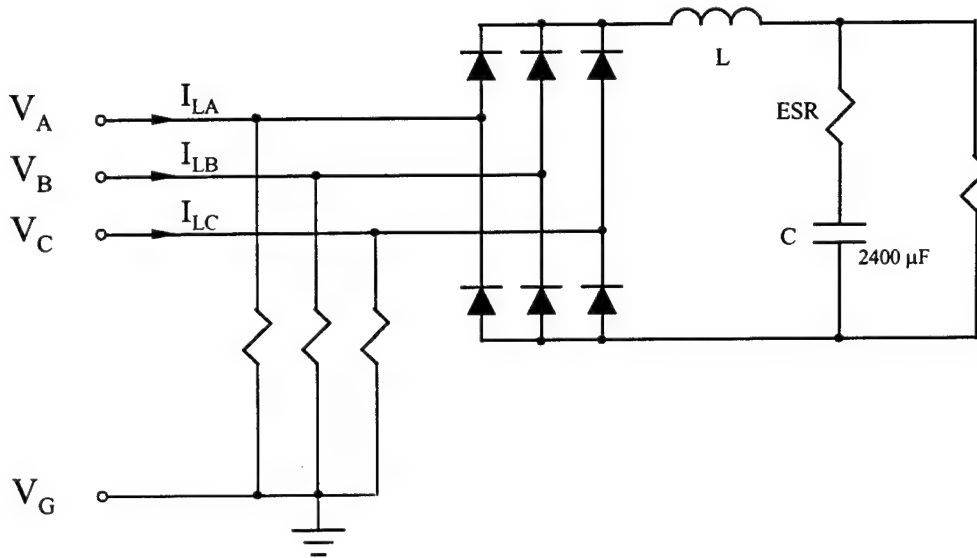
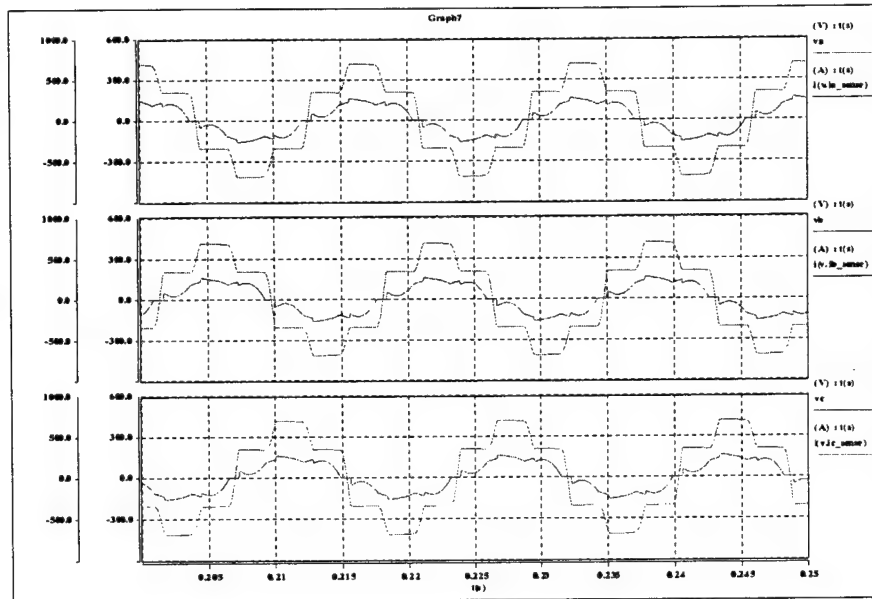


Figure 9-25. Tested nonlinear load.

The nonlinear loads are simulated. The simulation results with three-phase diode rectifiers with capacitor filter are shown in Figure 9-26 (a). It can be seen that the output voltages have several stairs, and are highly distorted. With an L/C filter, the output voltages are closer to sinusoidal. However, the voltage distortion is still very large. Three single-phase diode rectifiers with C filters and with L/C filters are simulated. The output voltage, load current and the neutral current are shown in Figure 9-27 (a) and (b). Due to the neutral triplen harmonics, the output voltages are close to square waves and heavily distorted. The overwhelming voltage distortion with nonlinear loads is caused by high output impedance at the frequencies of the harmonic currents.

(a)



(b)

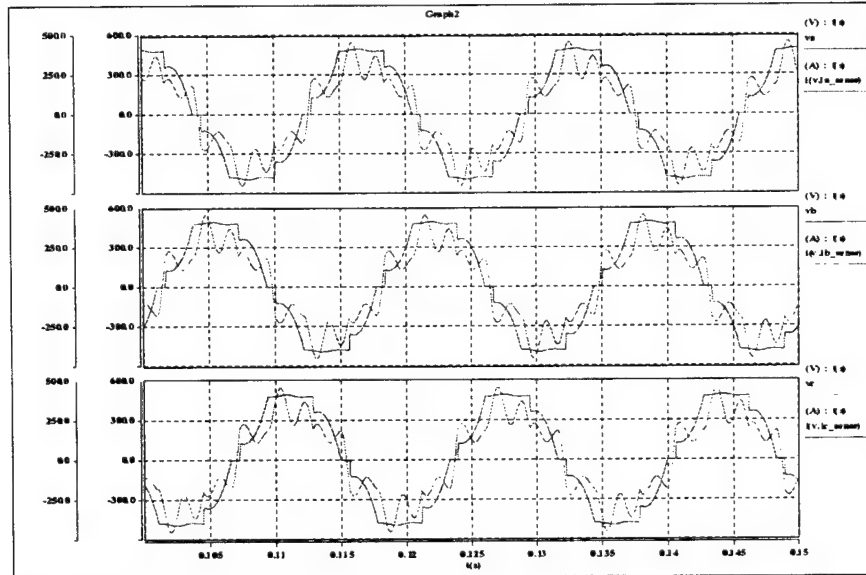
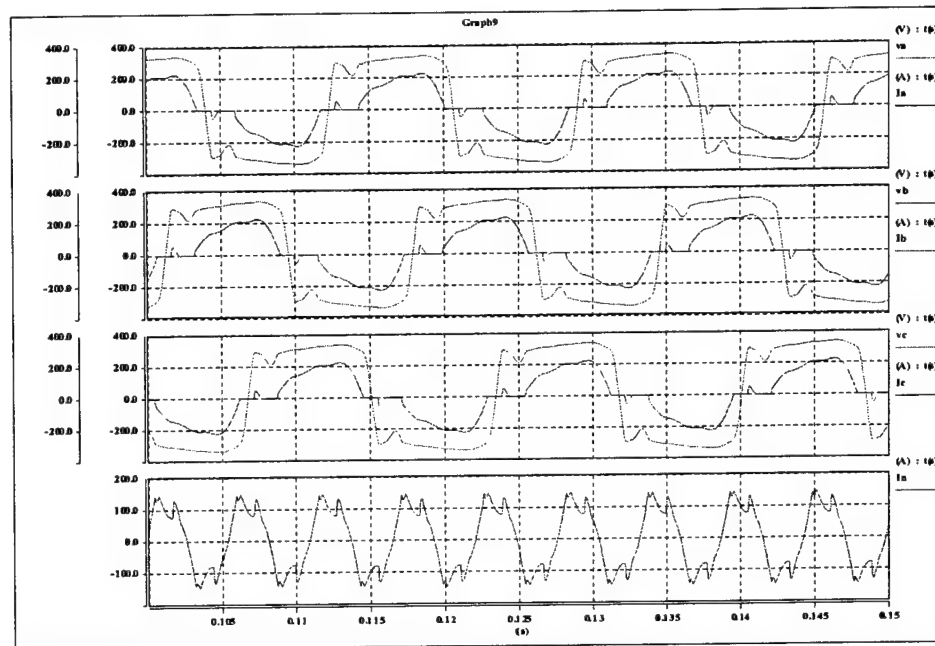


Figure 9-26. Simulated output voltages and load currents with voltage loop closed with three-phase diode bridge rectifier at 150 kW.

(a) with C filter. $C = 6900 \mu\text{F}$, $\text{ESR}_C = 150 \text{ m}\Omega$, $R = 2.67 \Omega$;

(b) with L/C filter. $L = 10 \text{ mH}$, $C = 6900 \mu\text{F}$, $R = 2.67 \Omega$

(a)



(b)

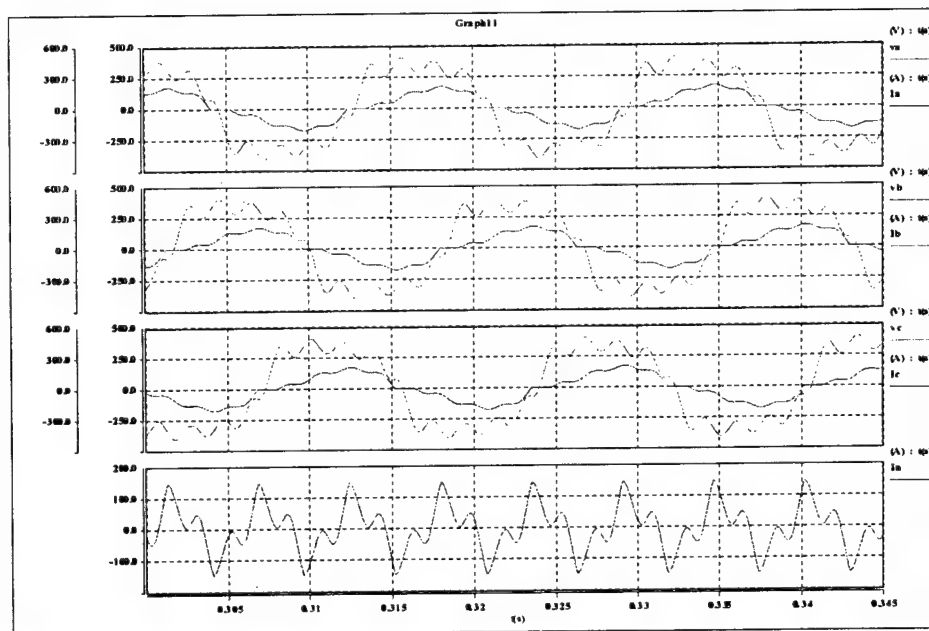


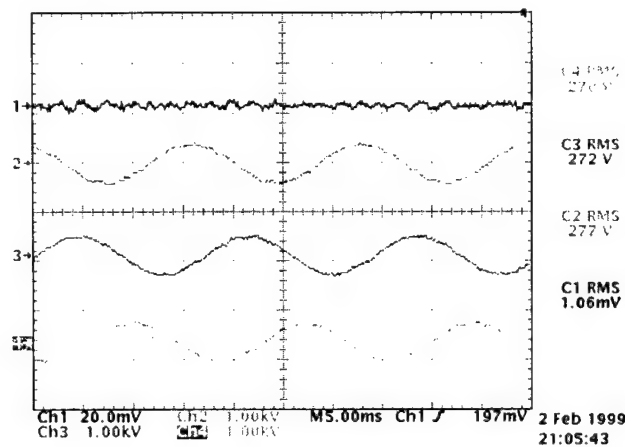
Figure 9-27. Simulated output voltages, load currents and neutral current with voltage loop closed with three single-phase diode bridge rectifiers at 150 kW.

- (a) with C filter. $C = 6900 \mu\text{F}$, $\text{ESR}_C = 250 \text{ m}\Omega$, $R = 2.7 \Omega$ per phase;
 (b) with L/C filter. $L = 1 \text{ mH}$, $C = 6900 \mu\text{F}$, $R = 2.7 \Omega$ per phase

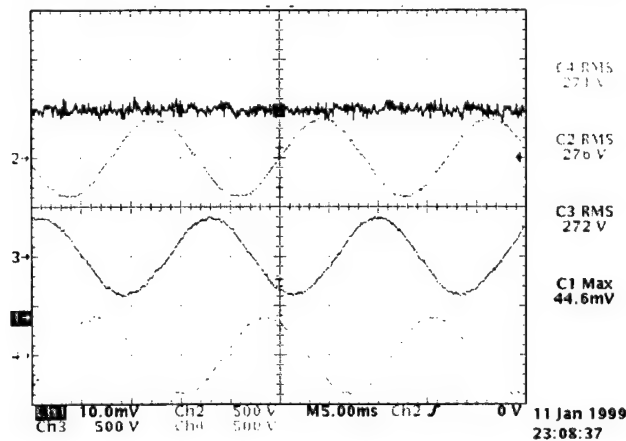
9.5.3 Experimental test results

9.5.3.1 Balanced resistive load case

With the designed voltage control loops, Figure 9-28 shows the measured output voltage and DC input line current with a balanced resistive load at 277 Vrms and 800 Vdc line input. Figure 9-28(a) shows the test case with $12.7\ \Omega$ load per-phase and channel 1 with AC couple to show the AC current ripple on DC bus. Figure 9-28(b) shows the test case with $3.1\ \Omega$ load per-phase and channel 1 with DC couple to show the overall current drawn from DC bus. Under the balanced resistive load case, the DC current ripple is small and the output voltage THD is 2.6%, which satisfies the design target.



(a) $12.7\ \Omega$ load each phase, channel 1 with AC couple



(b) $3.1\ \Omega$ load each phase, channel 1 with DC couple

Figure 9-28. Experimental results with balanced linear load with voltage loops closed.

(500 V/div, 20 A/div)

9.5.3.2 Unbalanced Resistive Load Case

An unbalanced linear load is tested with the voltage control loop closed. Phases A and B are connected to $3.2\ \Omega$ resistors. Phase C has no load. The DC link voltage is 800 V. The 277 V AC output voltages gives 86 A load currents for Phases A and B. Phase C current is zero since it is unloaded. With the proposed 3-D space vector, a three-phase sinusoidal output voltage is obtained. It is slightly unbalanced with only the voltage control loop closed, as shown in Figure 9-29. The 2ω current ripple on the DC bus is quite large under unbalanced load case.

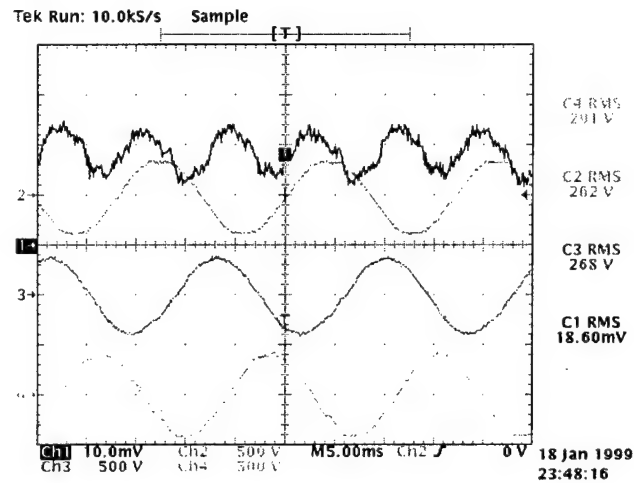


Figure 9-29. Experimental load current and DC bus current with an unbalanced linear load.

(500 V/div, 20 A/div)

9.5.3.3 Balanced nonlinear load case

A balanced nonlinear load is tested with the voltage control loop closed. Each phase is connected to a single-phase full-bridge rectifier with an LC filter followed by $12.7\ \Omega$ resistors. The filter consists of a $225\ \mu\text{H}$ inductor and a $260\ \mu\text{F}$ capacitor. The DC link voltage is 800 V and the output voltage is 137 Vrms. The tested waveforms are shown in Figure 9-30. Here the current channel 1 is AC coupled to measure the AC ripple on the DC bus. We can see that the output voltage waveforms have some distortion from the sinusoidal one and the current ripple on the DC bus is small under such balanced nonlinear load case.

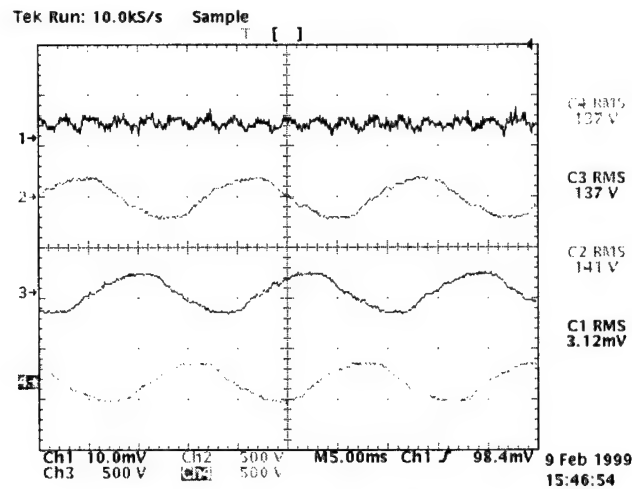


Figure 9-30. Experimental waveforms with a nonlinear load.
(500 V/div, 20 A/div)

9.5.3.4 Unbalanced nonlinear load case

Here an unbalanced nonlinear load is tested with the voltage control loop closed. Each phase is connected to a single-phase full-bridge rectifier with an LC filter. The filter consists of a 225 μH inductor and a 260 μF capacitor. For Phases A and B, the output of the filter is connected to a 6.3 Ω resistors, while for Phase C the output of the filter is not connected to any load. The DC link voltage is 800 V and the output voltage is 277 Vrms. The tested waveforms are shown in Figure 9-31. Here the current channel 1 is DC couple to measure the overall DC bus current. We can see that the output voltage waveforms have some distortion from the sinusoidal one and the current ripple on the DC bus is large. Furthermore, this DC bus current contains not only 2ω ripple but also other higher frequency ripple under such unbalanced nonlinear load case.

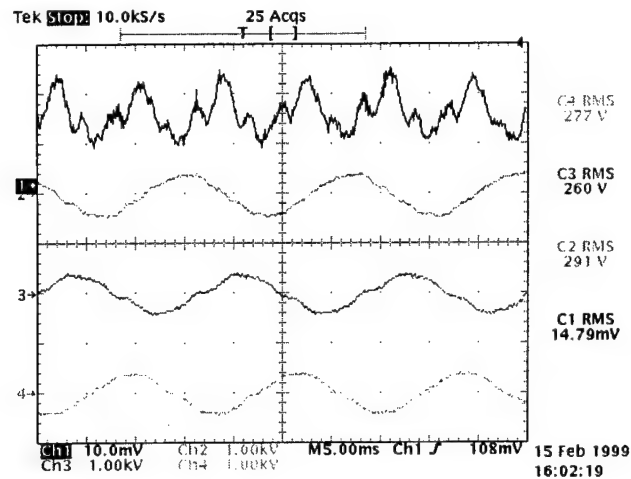


Figure 9-31. Experimental waveforms with an nonlinear load.
(1 kV/div, 20 A/div)

9.5.4 Summary

From both of the simulation and experimental results we find that using the proposed 3-D SVM and only the PI compensator for voltage control loop, with only the voltage loop closed, the four-leg inverter system can not deal with every kind of load. For unbalanced load case, the three-phase output voltage will get a little unbalanced and it cannot trap the 2ω current from entering the input DC bus. For nonlinear load case, the high-frequency current ripple will appear on the DC bus. These kinds of ripples can be used to study the system interaction issues and control issues in the whole PEBB system testbed. To solve the problems, a load conditioner and a DC bus conditioner are needed.

9.6 Conclusion

In this chapter, the different 3-D SVM schemes are introduced. The over-modulation issue in the 3-D SVM was brought up and explored. With the space geometrical analysis, the 3-D SVM over-modulation boundary is then defined as a hexahedron. Two over-modulation correction schemes are proposed to confine the SVM operation within the hexahedron. The proposed over-modulation schemes along with the system without over-modulation correction are compared with time-domain simulation and harmonic frequency analysis. With the proposed Scheme 1, the output voltage waveform quality can be improved, but distortion can be severe under unbalanced load condition. With the proposed Scheme 2, which confines the voltage vector to an inner surface, the voltage distortion can be nearly eliminated. However, its available magnitude is reduced.

Also, in this chapter, common mode EMI issues in 3-D SVM were brought up and discussed. Nine 3-D SVM schemes were investigated from EMI point of view. The SVM scheme selection is discussed. Of the nine schemes, the symmetrically aligned Class II scheme (SVM2) is the best selection.

Moreover, as part of the PEBB DC DPS testbed, one 100kW hardware setup was implemented and tested under 800 V rated DC bus voltage with several kind of load cases, including balanced/unbalanced, linear/nonlinear cases. From both of the simulation and experimental results we can find the effects of different load cases on the subsystem output and the input DC bus. The current ripple effects on the DC bus should be carefully considered when integrating the subsystem into the whole PEBB system since it may cause interaction and stability issues. However, further researches around this interaction problem can be carried out. To solve the problems, a load conditioner and a DC bus conditioner are needed.

9.7 Reference

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Chapter 10 A Three-Phase to Three-Phase Matrix Converter

10.1 Introduction

Matrix converter (MC) is a type of converter in which each output phase is directly connected to each input phase by one bi-directional semiconductor switch. It is a very hopeful candidate for the future power converter, because it has many ideal characteristics as the following.

- (a) Able to convert from any frequency to any frequency.
- (b) Sinusoidal waveforms on both output and input sides.
- (c) Unity or displaceable input power factor.
- (d) Highest efficiency.
- (e) No energy storage.
- (f) Bi-directional energy flow.

But there are some difficulties to implement MC.

- (A) Need many power devices
- (B) On-line computation of MC is too complex to be realized.
- (C) Commutation of bi-directional switches.
- (D) AC snubber, Protection, Shutdown are difficult.

There are many solutions to overcome these difficulties. Following section will very briefly discuss one of solutions we proposed.

10.2 Implementation

We are building a powerful (20KVA) MC to drive a motor system shown in Figure 10-1 for verifying all theories and techniques about MC in high power applications, and finding new issues and their solutions.

We use a kind of 6 in 1 IGBT module shown in Figure 10-1. And we are building a power block for one output phase, which includes one IGBT module, 6 gate drivers, a rectifier snubber, and an output current detector shown as in Figure 10-1.

We use a practical control method of MC that is almost as simple as that of inverter. It uses two instantaneous input voltages to compensate the effects of fluctuation, asymmetry or harmonics in the supply voltages on output voltages and input currents. Besides these, this method does not lose the advantages of other methods, such as 0.866 times output/input voltage ratio, sinusoidal input current and output voltage waveforms, displaceable input power factor.

We use the commutation sequences that are based on the output current direction because our snubber (see the followings) can protect the detecting miss for the output current direction.

In Figure 10-1, an AC snubber is shown that we call rectifier snubber. The capacitors in the rectifier snubber can absorb all voltage surges on all bi-directional switches, and on input side or output side of MC. V_{PN} is used as the DC source of all gate drivers. And there is a discharge circuit to discharge the capacitors through a resistor after V_{PN} is more than some value.

A protection system is built to sense such as input/output current over, low input voltage, snubber voltage over. If something happens, controller manages all switches to shutdown the MC as quickly as possible.

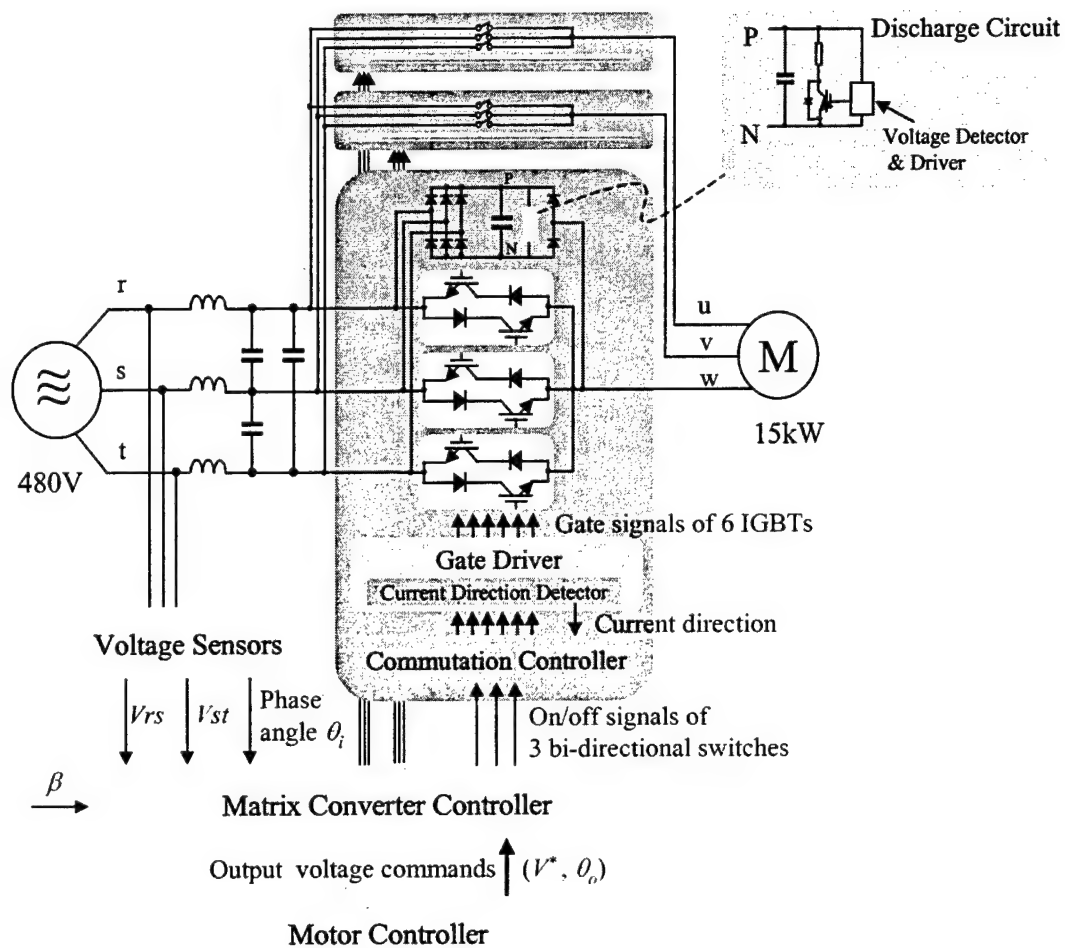


Figure 10-1. The system configuration of the matrix converter

Chapter 11 DC Bus Conditioner

11.1 The Concept of the DC Bus Conditioning

11.1.1 Introduction

In the process of the system integration, the greatest concern is the DC bus stability and system interaction. To ensure system stability, criteria need to be developed, and specifications have to be given to the “box” manufacturer. The minor loop gain concept – the ratio between the output impedance and the input impedance of the cascaded module – was introduced by Middlebrook in 1975 [1]. This is a very conservative criterion that requires a total separation between the input and output impedance at an interface, which may cause too much penalty or be too costly in the implementation. The gain margin and phase margin (GMPM) criterion was proposed by F. C. Lee et. al. It was adopted in the power system of the space station program [2-3,6]. This criterion allows for the overlap between the input and output impedance, but with a forbidden region for phase and gain reservation. Assumptions, which are unknown beforehand, have to be made before taking this concept down to the individual box level. Even with a well-defined criterion, a field design engineer may still face too many restrictions imposed by all the specifications in the practical design. For example, to design an input filter, all the constraints of filter damping, energy consumption, noise attenuation, output impedance and input impedance conflict with each other. In most cases, it is difficult to adjust the parameter to meet all the requirements. One natural question is whether we can shape the input impedance of a regulated power converter.

There is nothing more desirable than a load converter behaving resistively to the DC bus in a full frequency range in the small signal sense. On the other hand, the large signal input current characteristics of a power converter are equally important. The source converter expects DC current from the loads. But unfortunately, in most applications, there exists reactive and dynamic current on the DC bus because of pulsating loads, system transients, converters plugging in and off, possible system resonance, and so on.

The large signal harmonic interaction related to the unbalanced load and the small signal impedance interaction.

This chapter proposes a DC bus conditioner for a distributed power system. The system consists of a source converter, a DC bus conditioner and load converters. The load current on the DC bus can be divided into two categories: the DC component related to the active power, and the AC components representing the reactive power. The DC component, which encompasses a large percentage of the overall system power, is assigned to the source converter. The reactive power, which may take only a fraction of the total power, is assigned separately to the DC bus conditioner. Limited by a higher power rating, the source converter's switching frequency is relatively low. The system bandwidth can cover only the lower frequency range, whereas the bus conditioner processes less power and switches at higher frequency, and therefore has higher system bandwidth to deal with high-order system dynamics and high-frequency components. The DC bus conditioner contributes to the DC system in several ways. First, it shunts the large signal harmonic current from the DC bus. This is done through extra energy storage. Whenever the ripple current is needed, it will circulate through the bus conditioner, not to the bus. Second, it improves the transient dynamic response of the system because of its higher system bandwidth. Third, it helps to maintain the bus stability. The small signal analysis shows that the bus conditioner can boost the input impedance of the regulated converter in the middle frequency range where the interaction normally happens. The concept of the bus conditioner is illustrated in Figure 11-1.

11.1.2 The Circuit Structure for DC Bus Conditioner

There are two basic circuit topologies that can be used for the DC bus conditioner. One is the capacitor energy storage type. The other is the inductor energy storage type. The capacitor energy storage bus conditioner is shown in Figure 11-2. This is a boost-buck structure with an input inductor, a PEBB module and an energy storage capacitor. In boost-mode operation, the bottom switch and top diode of the phase-leg are activated. The storage capacitor absorbs the energy from the DC bus. In buck mode operation, the top switch and bottom diode will be activated. The energy storage capacitor releases

energy back to the bus. Its purpose is to shunt the AC current into a capacitor that is not connected directly to the bus, thus isolating the DC bus from the ripple current contamination. The energy storage capacitor can be small, because there is no other load on it and, therefore, it tolerates a higher voltage ripple.

The bus conditioner is essentially a current-controlled current source. At the critical load points, it senses the load current. A band-pass filter is used to determine the frequency range in which it should respond. The lower end of the passing band will determine the maximum energy storage, because the low-frequency current usually contains higher energy. Its higher end is limited by the current loop bandwidth, or, in other words, the switching frequency. The output of the bandpass filter is used as the reference signal for the current loop. The duty cycles are generated to control the current to the opposite polarity as the AC current on the DC bus. In system transients, the DC bus conditioner responds quickly to provide the transient energy momentarily. A very slow voltage loop is used to put extra control on the duty cycles to make up the system energy loss/gain in transients. This also maintains the energy level on the capacitor in system quiescent state. Its bandwidth is low enough not to disturb the operation of the current loop at transients.

11.2 Design and Control Considerations

11.2.1 Component Selection

The selection of the components in the bus conditioner depends on the application. The essential factors are power rating and switch frequency and system bandwidth requirements. The circuit topologies can be derived based on the basic configurations. For example, the voltage on the energy storage capacitor is higher than the DC bus voltage in order to be able to transfer energy back to the DC bus. If the DC bus voltage itself is very high, three-level circuit topology can be used, as shown later in Section 4.

The following shows the design considerations for the capacitor type bus conditioner.

Assume the DC bus voltage is V_{dc} ; the circulating power between the bus conditioner and the DC bus is P_o , and the major concerned AC current is I_{ac} in Hz.

The average current of the circulating power will be:

$$I_{avg} = \frac{P_o}{V_{dc}} \quad (5-1)$$

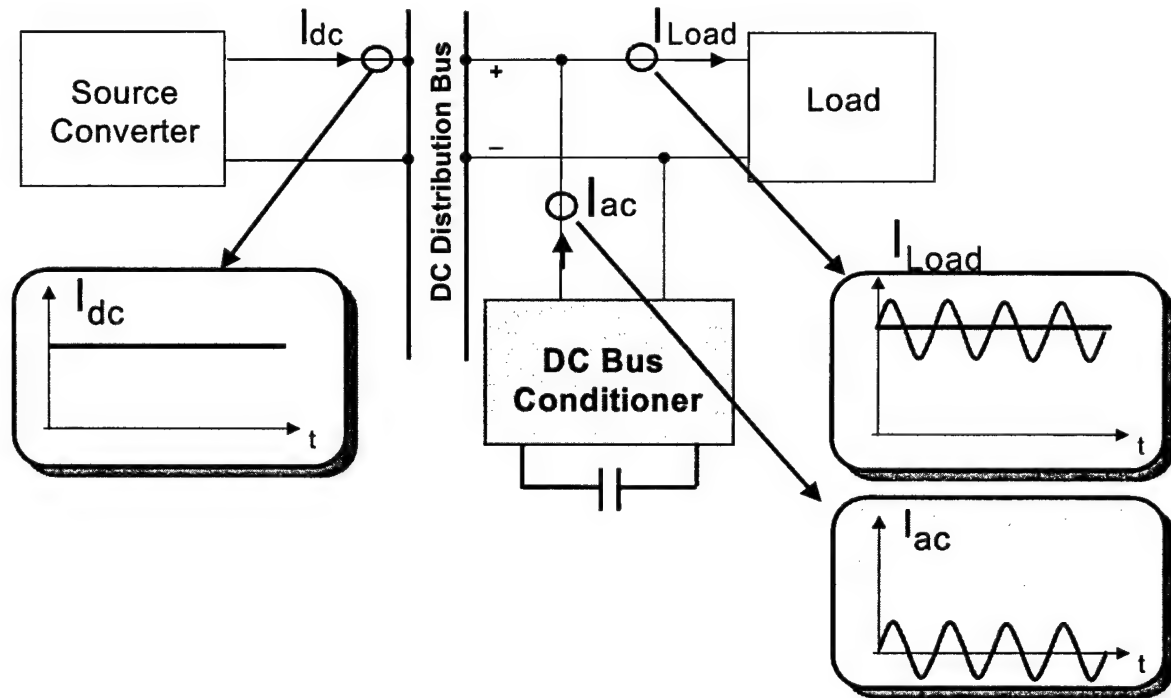


Figure 11-1. The concept of active bus conditioner.

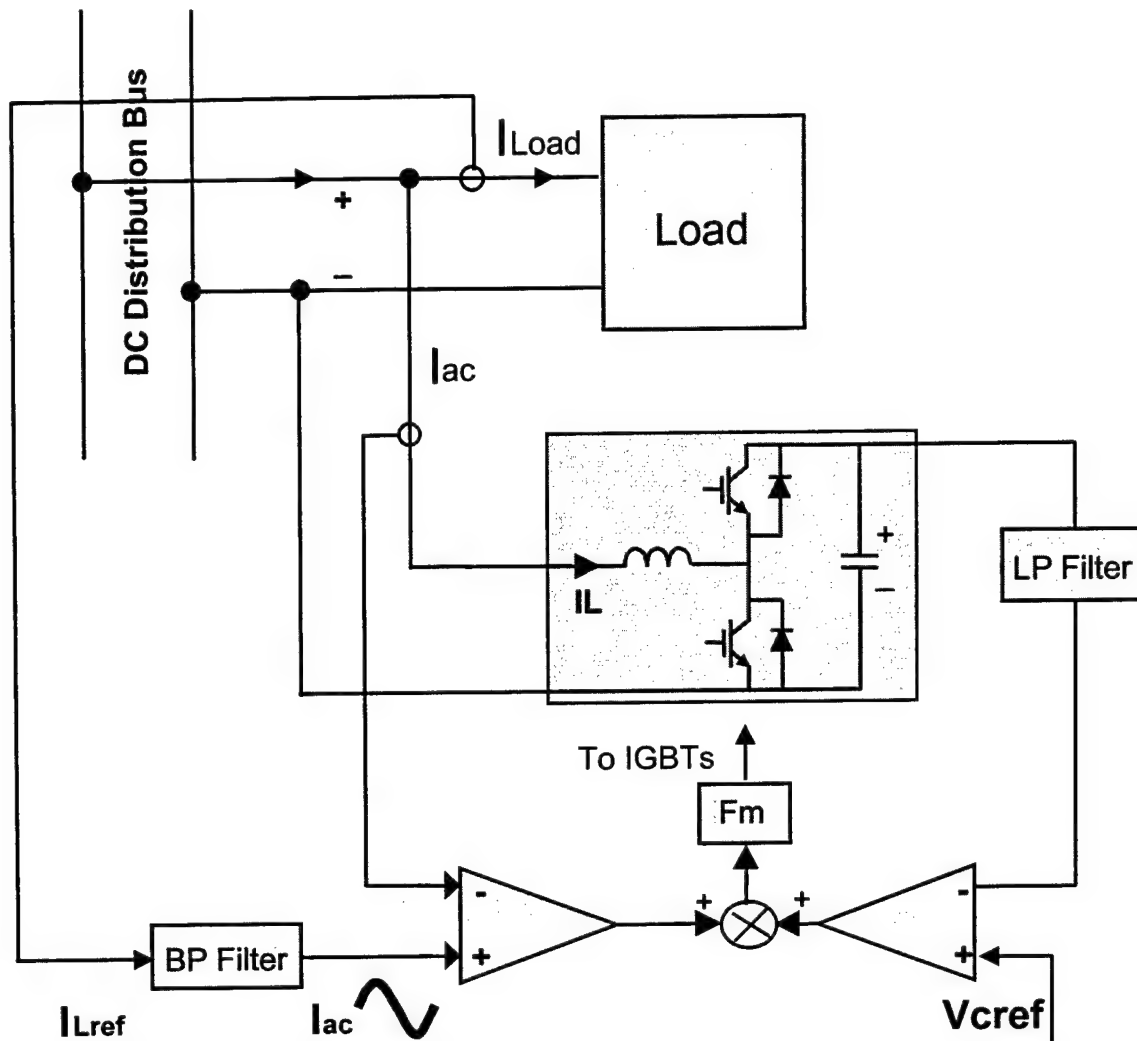


Figure 11-2. The capacitor type conditioner and its control function blocks.

This current is equivalent to a sinusoidal current I_{ac} :

$$I_{avg} = \frac{1}{\pi} \int_0^{\pi} I_{ac} \sqrt{2} \sin(\omega_{ac} t) d\omega_{ac} t = \frac{2\sqrt{2}}{\pi} I_{ac} \quad (5-2)$$

The value of I_{ac} can be used as the reference of the current rating of the active devices plus other factors such as current ripple. The voltage rating selection of the active device is straightforward depending on the voltage level on the energy storage capacitor. The major design consideration of the active device is the thermal management associated with high switching frequency.

First of all, the maximum power dissipation capability of the circuit depends on the heat sink selection. If the temperature difference between the case of the active device and its junction temperature is ΔT_{cj} :

$$\Delta T_{cj} = T_j - T_c \quad (5-3)$$

The maximum allowed power loss dissipation for the active device will be:

$$Pd = \frac{\Delta T_{cj}}{R_{th_{cj}}} \quad (5-4)$$

where $R_{th_{cj}}$ is the thermal resistance of the active device, which is a function of the die size and the packaging technology. At the desired switching frequency of f_s , the total power loss of the active device will be:

$$Pd = F(f_s) = (E_{on} + E_{off})f_s + P_c \quad (5-5)$$

In equation (5-5), E_{on} and E_{off} are the turn-on and the turn-off energy of the selected device at the normal operation condition. P_c is the conduction loss of the device. They can be found in the device data sheet or the real device burn test. The device selection is a trial-and-error process. The thermal resistance, turn-on and turn-off energy, and conduction loss of the selected device have to meet the equation (5-5) at a given switching frequency, input and output voltage and current and other operation conditions.

Selection of the capacitor is a trade-off of maximum allowed voltage ripple and the capacitance. The larger the capacitance, the easier the control, the less voltage ripple in the system dynamics, and of course, the higher the cost.

The total charge that is going to be pumped into the capacitor in half AC current cycle is:

$$Q = \frac{I_{avg}}{2F_{ac}} \quad (5-6)$$

The voltage variation on the capacitor with this amount of charge is:

$$\Delta V_c = \frac{Q}{C} \quad (5-7)$$

There are two major AC current components going into or out of the capacitor. One is the harmonic current frequency on the DC bus, and the other is the switching frequency. The ESR of the capacitor is chosen to be very small in all the frequency ranges in order to reduce the power loss, which is a function of the square of the RMS current.

There are also two major considerations for inductor design. One is current ripple under the given switching frequency. The other is the delay effect between the real AC current and the inductor current. Under system transients, inductor current has to provide the desired current slew rate required by the load. The ripple current as a function of the switching frequency is:

$$\Delta i_L = \frac{V_{dc} D}{L F_s I_{ac} \sqrt{2}} (\%) \quad (5-8)$$

In Equation (5-8), the D is the duty cycle. If the voltage on the storage capacitor is two times higher than the DC bus voltage, the steady state duty cycle will be about fifty percent.

11.2.2 Modeling and Control of the DC Bus Conditioner

There are three basic function blocks in the control loop, the band pass filter, the high bandwidth current loop, and the low bandwidth voltage loop. The band pass filter provides the reference signal to the current loop.

11.2.2.1 Design of the Band Pass Filter

The most important design criteria of the band pass filter are the cut-off frequency and the phase delay. An ideal filter would provide unity gain and zero phase delay in its passing band and much higher attenuation at the blocking band. A very convenient way to construct a band pass filter is to use two low pass filters with one at low cut-off frequency and one at high cut-off frequency and combine them at their output. Second order filters were used:

$$FL1(s) = \frac{1}{\left(\frac{s}{\omega_1}\right)^2 + \xi_1 \frac{s}{\omega_1} + 1} \quad (5-9)$$

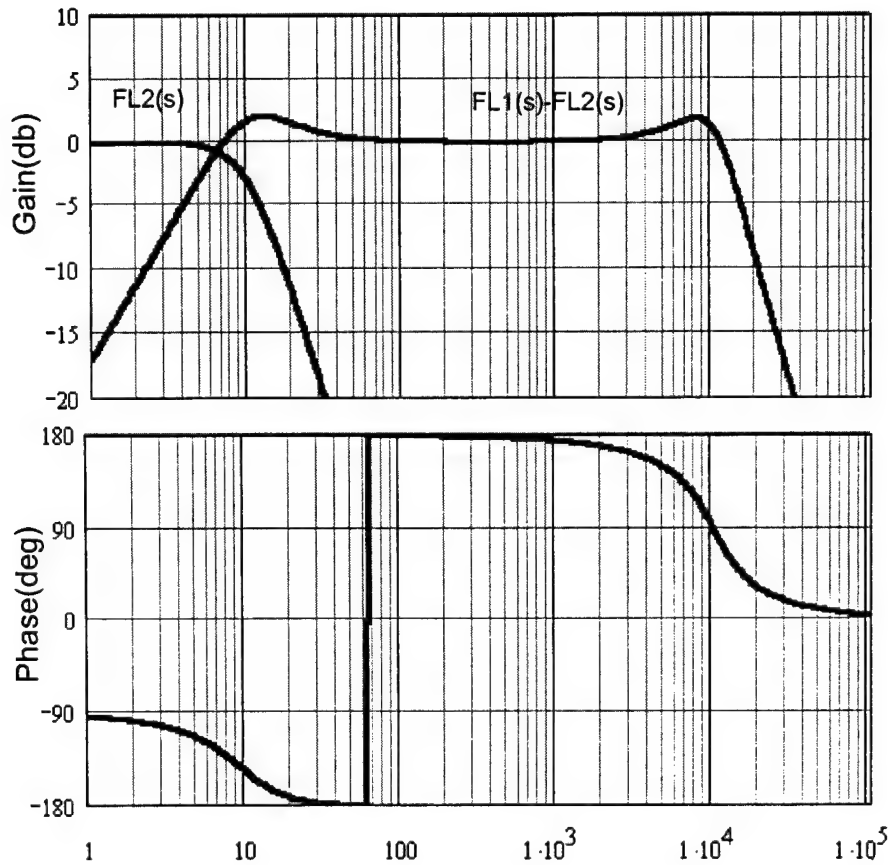


Figure 11-3. Band pass filter design.

$$FL2(s) = \frac{1}{\left(\frac{s}{\omega_2}\right)^2 + \xi_2 \frac{s}{\omega_2} + 1} \quad (5-10)$$

$$FL(s) = FL1(s) - FL2(s) \quad (5-11)$$

The design example is shown in Figure 11-3. FL1(s) is the low pass filter with a 10 kHz cut-off frequency. FL2(s) is the one with a 10 Hz cut-off frequency. The combined filter shows a passing band from 100 Hz up to 4 kHz. Generally, a distribution system will have a characteristic frequency on which either the oscillation is most likely to happen or the load harmonics current exists. The inverter load might bring 2ω frequency into the

system. The band pass filter is designed to pick up this characteristic frequency in the distribution system with high fidelity, and let the bus conditioner produce a counter current to balance the oscillation or the harmonic current.

11.2.2.2 Derivation of the Plant Transfer Function

The average model of the half-bridge PEBB module can be used directly for the bus conditioner. The DC bus conditioner operates like a single-phase power factor correction circuit in a way that the inductor current is not constant like in a DC/DC converter. The small signal analysis method used for the PFC circuit design can be applied to the bus conditioner also. The system control block diagram is shown in Figure 11-4. The transfer functions from duty cycle to inductor current and from the duty cycle to capacitor voltage can be obtained based on the averaged PEBB model.

$$Fi(s) = \frac{\hat{IL}}{\hat{d}} = \frac{IL}{D} \frac{(s/wz + 1)}{as^2 + bs + 1} \quad (5-12)$$

$$Fv(s) = \frac{\hat{Vc}}{\hat{d}} = \frac{R_L IL - DVc}{D^2} \left(\frac{(s/wz1 + 1)(s/wz2 + 1)}{as^2 + bs + 1} \right) \quad (5-13)$$

In equation (5-12) and (5-13)

$$a = \frac{LC}{D^2} \text{ and } b = \left(\frac{R_L}{D^2} + Rc \right) C$$

The duty cycle to the inductor current transfer function has a DC gain of IL/D , a zero at very low-frequency which is not a concern for the current loop that is supposed to operate at high-frequency only, and double poles at the LC resonant frequency. Actually, the bus conditioner resembles the audio amplifier; any AC current falling in its passing band will be reproduced counter-wise. As that of the linear amplifier, the DC bus capacitor and the energy storage capacitor can be treated as a short-circuit in high-frequency small signal analysis. The high-frequency characteristics of $Fi(s)$ can be approximated as:

$$\frac{\hat{IL}}{\hat{d}} \approx \frac{V_c}{sL} \quad (5-14)$$

The duty cycle to capacitor voltage has a DC gain, two zeros at very high-frequency, and two system double poles. The high-frequency zero is not a concern for voltage loop design, because the voltage loop operates at very low-frequency. The duty cycle to inductor current transfer function is shown in Figure 11-5. The duty cycle to capacitor voltage transfer function is shown in Figure 11-6. The high-frequency zero effect can be seen in the phase of diagram of the Bode plot.

11.2.2.3 Design of the current and voltage loop controller

In the system control block diagram in Figure 4, there are two paths of signal flow. One is the low-frequency path, which is the voltage loop. The other is the high-frequency path, which is the current loop. The system can be analyzed separately. The procedure of control design is straightforward as long as the plant transfer function becomes known. From the control diagram, the transfer function from the inductor current reference to the real inductor current can be obtained:

$$\frac{\hat{IL}}{\hat{IL}_{ref}} = -\frac{Fi(s)Fm}{1+Ti}(FL2(s)-FL1(s)) \quad (5-15)$$

In equation (5-15), Ti is the current loop gain. And $Ci(s)$ is the current loop compensator.

$$Ti = Gi(s)RiHe(s)Ci(s)Fm \quad (5-16)$$

Figure 11-7 shows the Bode plot of the transfer function from the reference signal to the inductor current with a proportional controller. The current loop together with the band pass filter constructs a good passing band from 100 Hz to 4 kHz. Within the passing band, the bus conditioner has a unity gain and phase of 180 degrees. It will produce the counter balance current to the DC bus.



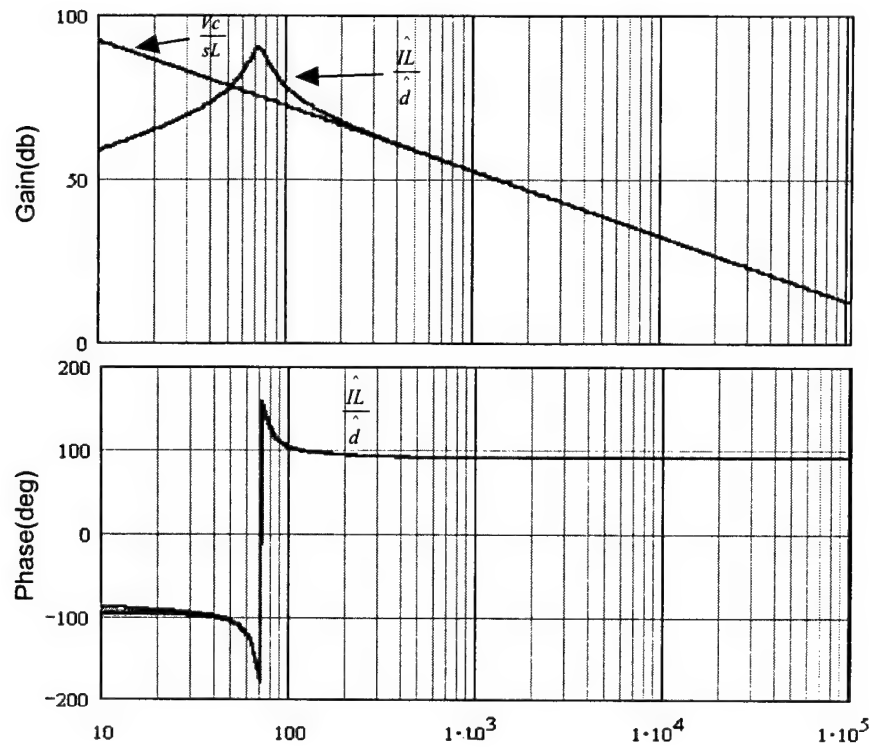


Figure 11-5. The Bode plot of the duty cycle to inductor current transfer function.

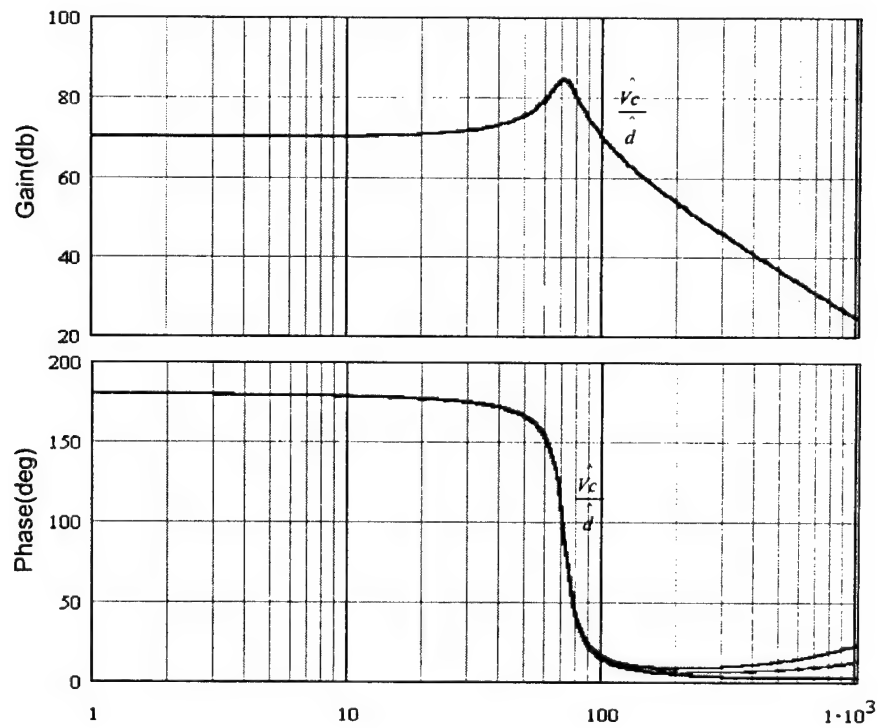


Figure 11-6. The Bode plot of the duty cycle to capacitor voltage transfer function.

A simple integrator with a low-frequency pole, which attenuates the low-frequency ripple voltage on the capacitor, can be used for the voltage loop. The voltage loop has two functions. One is to maintain a certain amount of energy storage on the capacitor, and the other is to buffer the high-frequency current transient into low-frequency dynamics. It has a very narrow bandwidth. The voltage loop gain is plotted in Figure 11-8.

11.2.2.4 The Inductor Type Circuit

The inductor energy storage type circuit is shown Figure 11-9. It is a bi-directional chopper with an energy storage inductor. The inductor is pre-charged with a certain amount of energy. If the on-times of the two active switches are equal to the on-times of the diodes, there will be no effective energy transfer between the inductor and the DC bus. If the on-time of the active switch is longer than the on-time of the diodes, the energy is transferred to the inductor and vice versa. By controlling the duty cycle, the ripple current is absorbed to the inductor, not the DC bus.

The control of the inductor type circuit is similar to that of the capacitor-type circuit. It has a high bandwidth current loop to track the AC current from the load and a slow current to regulate the average current, or the energy storage, of the inductor.

The voltage rating of the semiconductor device in a capacitor-type circuit is higher than that of the inductor type. The input current of the capacitor-type circuit is continuous because there is an inductor at the input side, whereas the input current of the inductor type circuit is pulsating. It has switching frequency ripple. An input filter is desirable to smooth the ripple current, but it may bring extra phase shift and degrade the performance of the bus conditioner. Another consideration is that a capacitor may have a higher energy density at high voltage than the inductor. For a given amount of the energy E , the relationships between the capacitance and inductance are given by:

$$E = \frac{1}{2}CV^2 = \frac{1}{2}LI^2 \quad (5-17)$$

In applications where the big inductor is available, the inductor type bus conditioner can be used. One of the big advantages of the inductor type circuit is that it is able to provide very high di/dt slew rate compared to the capacitor type circuit.

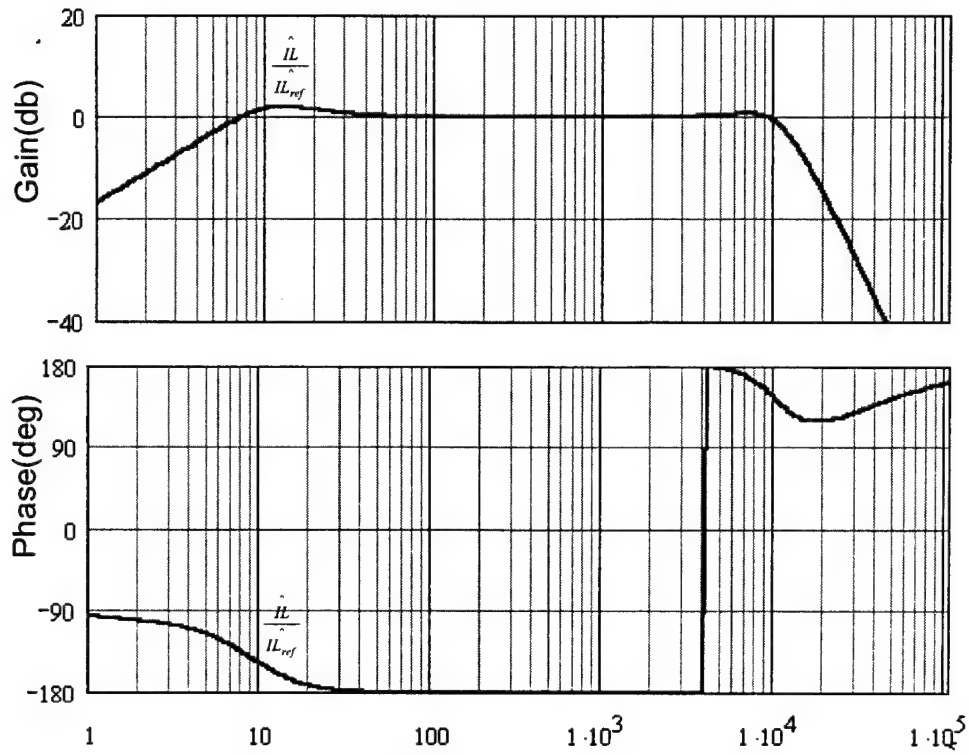


Figure 11-7. The Bode plot of the transfer function from the load AC signal to the inductor current.

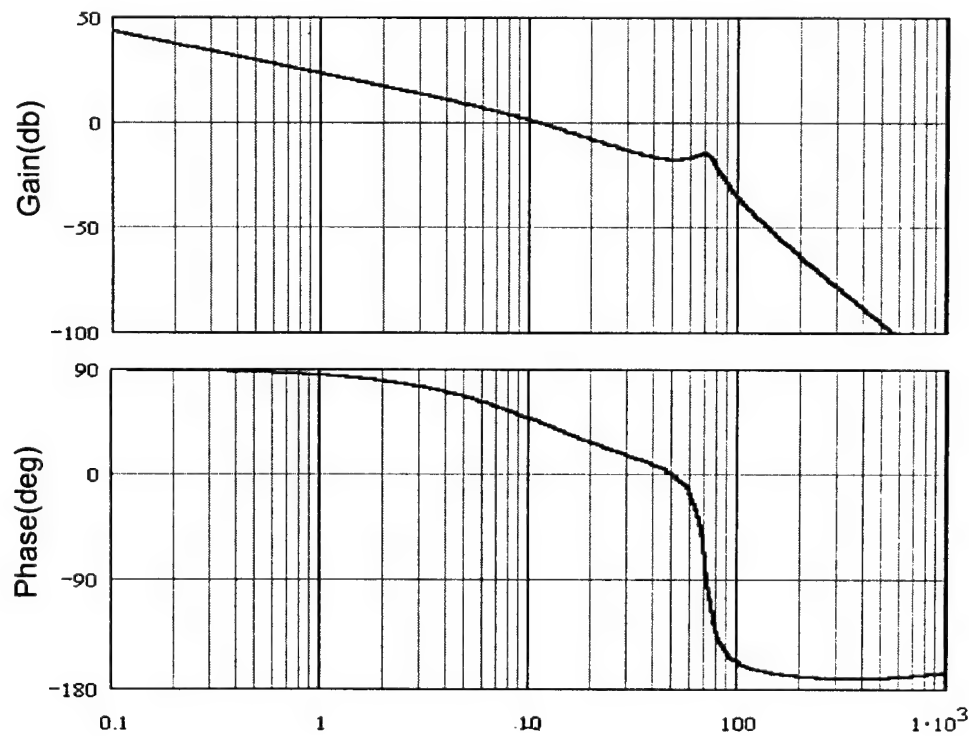


Figure 11-8. Bode plot of the voltage loop gain.

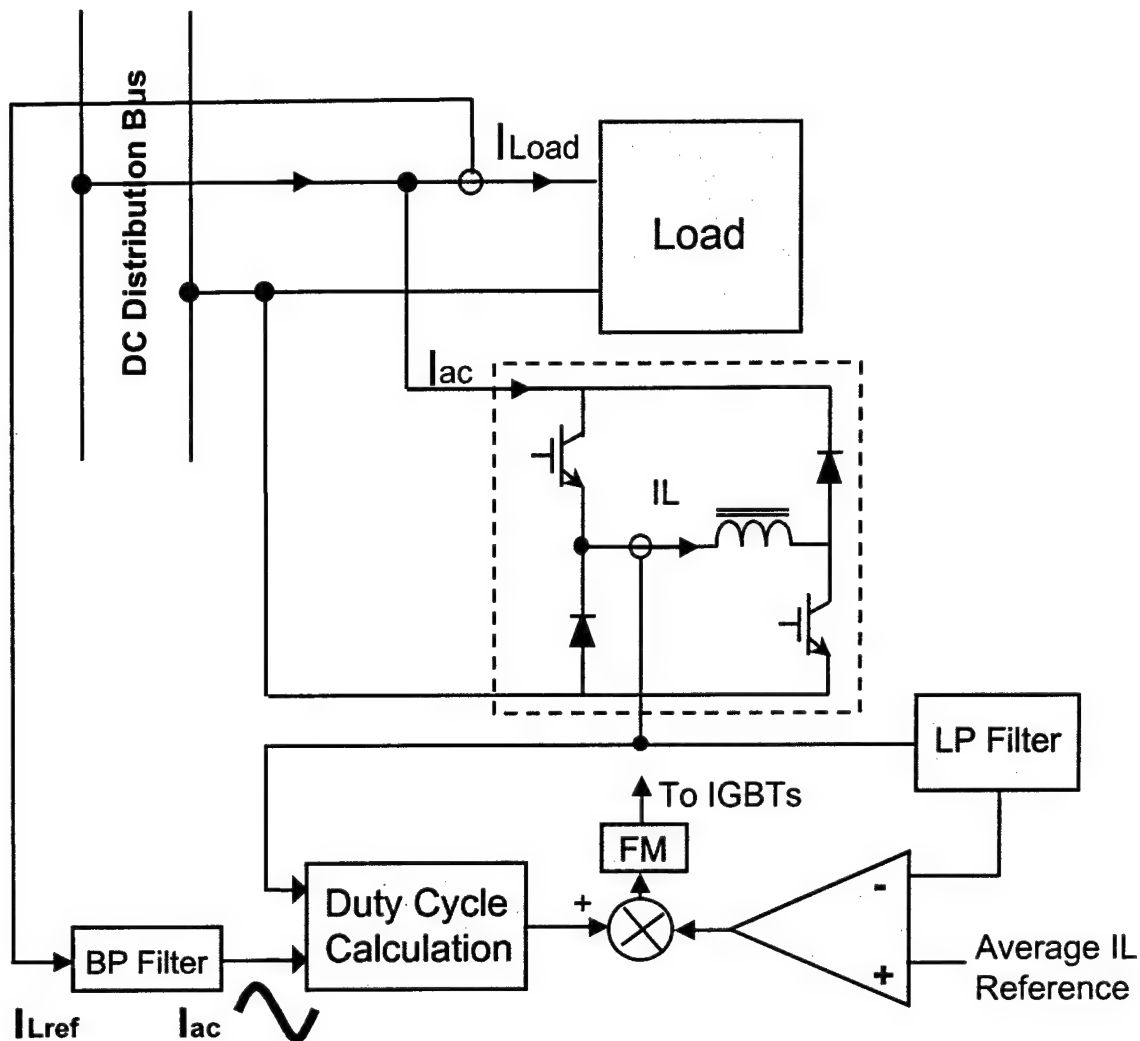


Figure 11-9. The inductor type DC bus conditioner with its control blocks.

There are three different operational modes of the circuit: the charge mode, the discharge mode, and the freewheeling mode. In the charge mode, all the active switches are on. The DC bus voltage is applied directly to the inductor. The inductor absorbs energy from the DC bus. In discharge mode, all the active switches are off, and the inductor current discharges from the diode branches to the DC bus. It releases energy back to the bus. In freewheeling mode, only one of the active switches is on, either the top or the bottom. The current circulates inside the circuit through one active device and one diode. There are losses produced by the voltage drop of the semiconductor devices and the conductors in freewheeling mode.

The large signal average model can be derived based on the charging duty cycle as shown in Figure 11-10. The small signal characteristics of the circuit can be obtained based on the average model.

Because the current generated by the bus conditioner is pulse-width-modulated, a PWM voltage waveform will be applied to the inductor. If the inductor is not large enough, a current ripple could be excited. This will affect the input current modulation in turn. In this case the inductor current ripple effect has to be compensated on-line, which is shown in Figure 11-11. The rule for the duty cycle compensation is:

$$De = \frac{I_{ref}}{IL_{avg} + I_{ripple}} \quad (5-18)$$

De is the effective duty cycle. Using the instantaneous inductor current to compensate the duty cycle is a viable approach to use small inductor and allow relative high current ripple on the inductor.

11.3 The Functions of the DC Bus Conditioner

The function of the bus conditioner is demonstrated through examples as shown in the following.

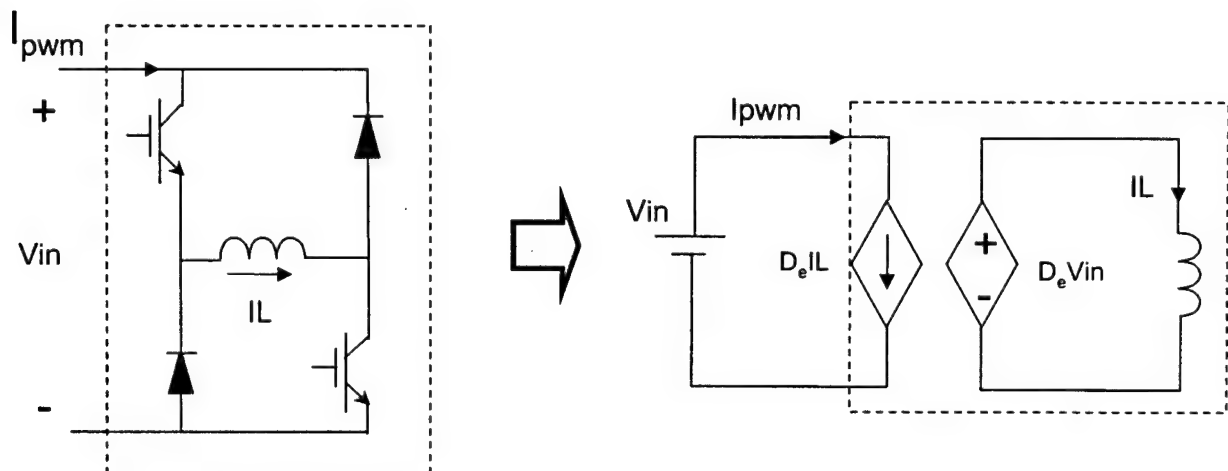


Figure 11-10. The average model of the inductor type current.

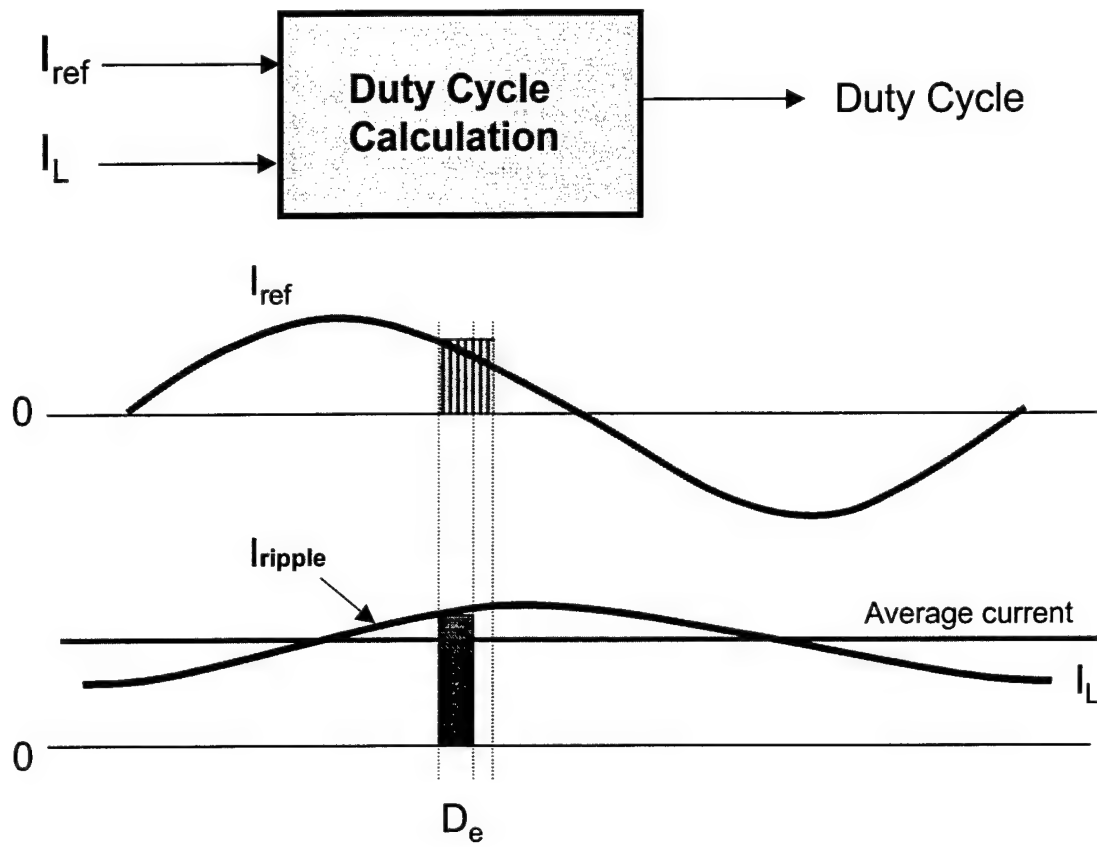
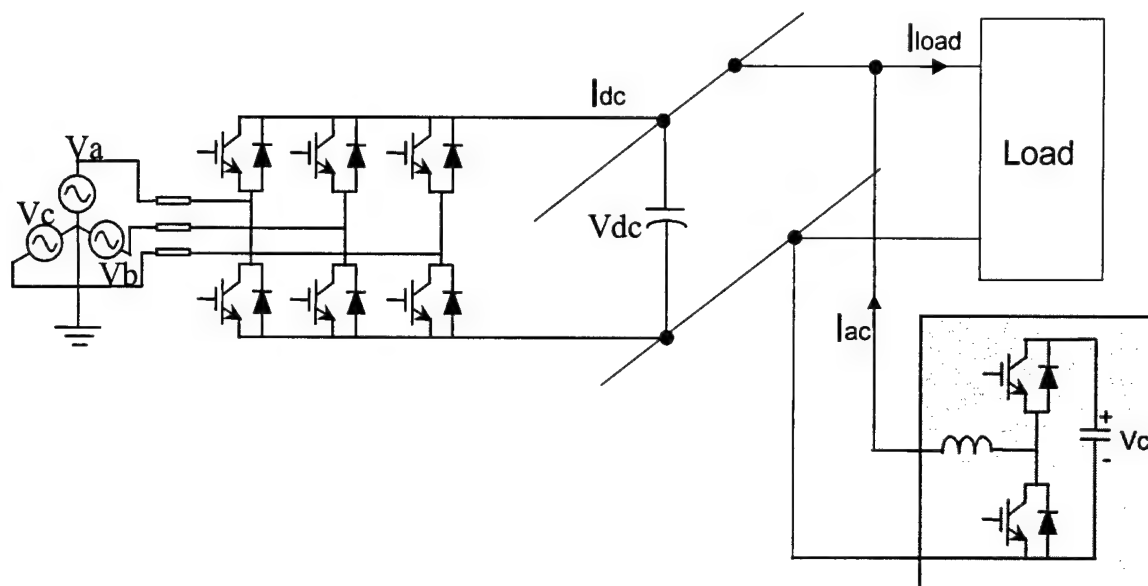
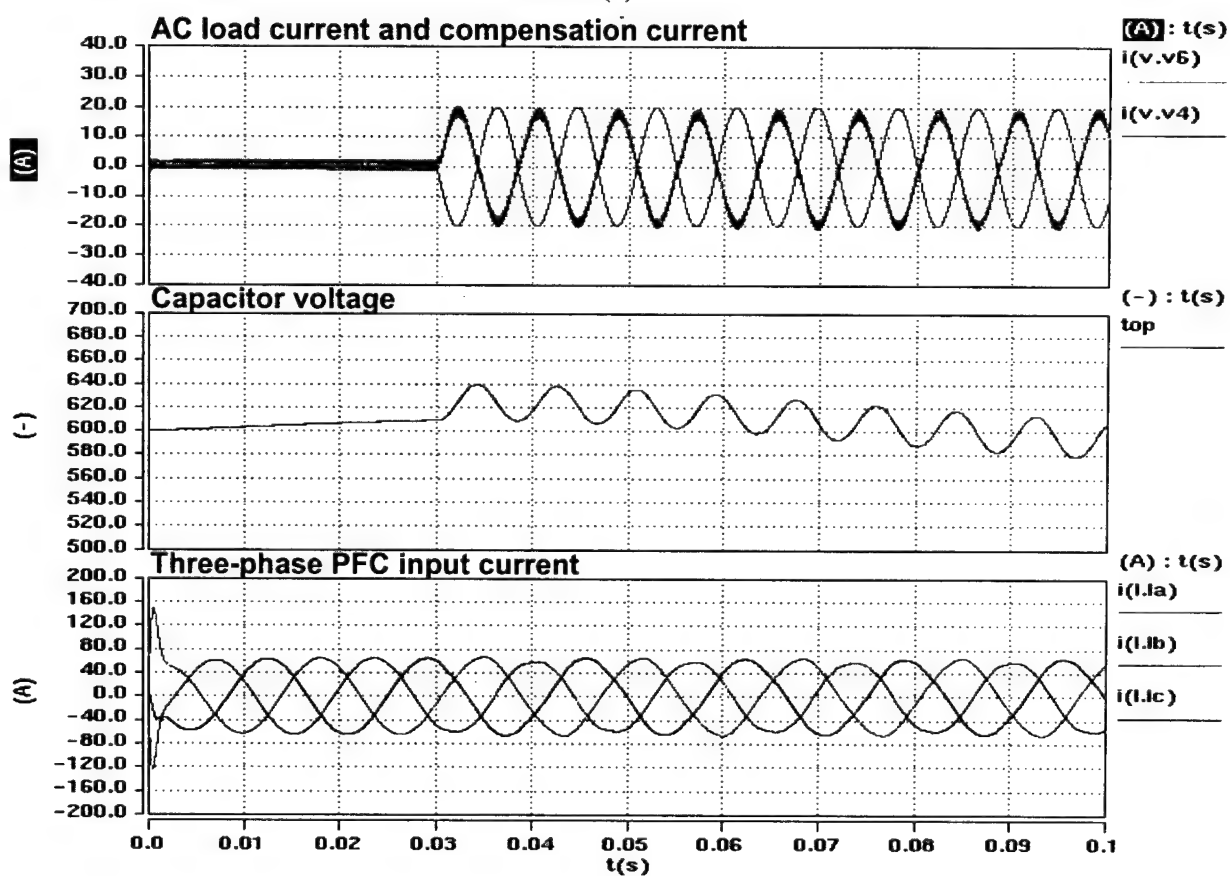


Figure 11-11. Compensation of the duty cycle according to the current ripple.



(a)



(b)

Figure 11-12. The bus conditioner connected with pulsating load to provide the harmonic current.

11.3.1 Providing the Harmonic Current of the Pulsating Load

The system connection diagram is shown in Figure 11-12. An inverter load draws 2ω ripple current from the DC bus. The bus conditioner is connected at the input point of the inverter. In this system, the bus conditioner provides the AC harmonic current as required by the pulsating load. As shown in the waveform, when the pulsating current is injected into the system, the DC bus conditioner produces a current with opposite direction. The bus voltage still remains regulated by the rectifier. The three-phase PWM rectifier is not affected by the pulsating load, and the three-phase input current is immune from the distortion. The energy storage capacitor takes over the pulsating current; therefore, its voltage has the ripple content.

11.3.2 Buffering the System Dynamics

The system dynamic response can become very oscillatory when the input and output impedance of rectifier and inverter load are very close to each other. The bus conditioner now is connected on the DC bus source converter is the three-phase rectifier with an input of 480 V, and the DC bus voltage 800 V. The load is a four-leg inverter for secondary utility power supply. When a step load is applied at the output of the four-leg inverter, there will be current step change reflected to the DC bus. With the help of the DC bus conditioner, the very fast transient current is diverted to the energy storage capacitor. Therefore, the bus voltage does not change significantly, it dips only 4.6 V compared to 48 V before. In the transient process, the capacitor is discharged. The voltage loop of the bus conditioner slowly adds control on the duty cycle and charging the energy back to the capacitor.

11.3.3 Improving the Load Input Impedance / Source Output Impedance

The impedance measurement setup diagram is shown in Figure 11-14. A small signal current perturbation is applied to the DC bus. While the bus voltage responds to the perturbation, the current is shared among different boxes. The source output impedance and load input impedance of the boxes on the DC bus are:

$$Z_s = \frac{\hat{V}_{bs}}{\hat{i}_s} \quad (5-19)$$

$$Z_L = \frac{\hat{V}_{bs}}{\hat{i}_L} \quad (5-20)$$

Because the bus conditioner is a current follower, the perturbation current going into the load will be replicated in its passing band.

$$\hat{i}_{bc} \approx -\hat{i}_L \quad (5-21)$$

The equivalent load current including the bus conditioner will be:

$$\hat{i}_{Le} = \hat{i}_s + \hat{i}_L \approx 0 \quad (5-22)$$

Therefore, the combined input impedance becomes very high.

$$Z_{Le} = \frac{\hat{V}_{bs}}{\hat{i}_{Le}} \quad (5-23)$$

As shown in Figure 11-14, the equivalent input impedance looking into the shaded box is boosted up by over 30 dB in its active region compared to the impedance without the bus conditioner. The equivalent impedance still shows the regulated converter at a very low-frequency with its phase starting at minus 180 degrees. Once inside the DC bus conditioner's active range, the phase rises rapidly to zero. Meanwhile, it successfully accomplishes a wide separation with the output impedance of the input filter.

The DC bus conditioner can be treated as part of the source from the other point of view. The equivalent source impedance can be defined as the ratio between the bus voltage and the total current of source and the DC bus conditioner:

$$Z_{se} = \frac{\hat{V}_{bs}}{\hat{i}_{se}} = \frac{\hat{V}_{bs}}{\hat{i}_s + \hat{i}_{bc}}$$

The equivalent source impedance will be reduced in the active region of the bus conditioner.

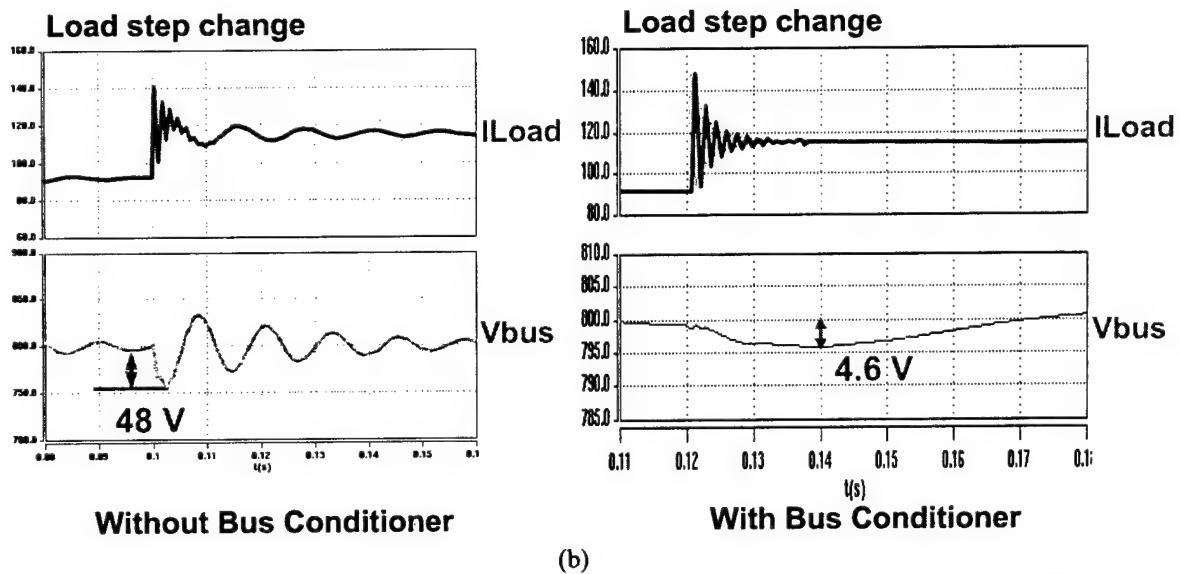
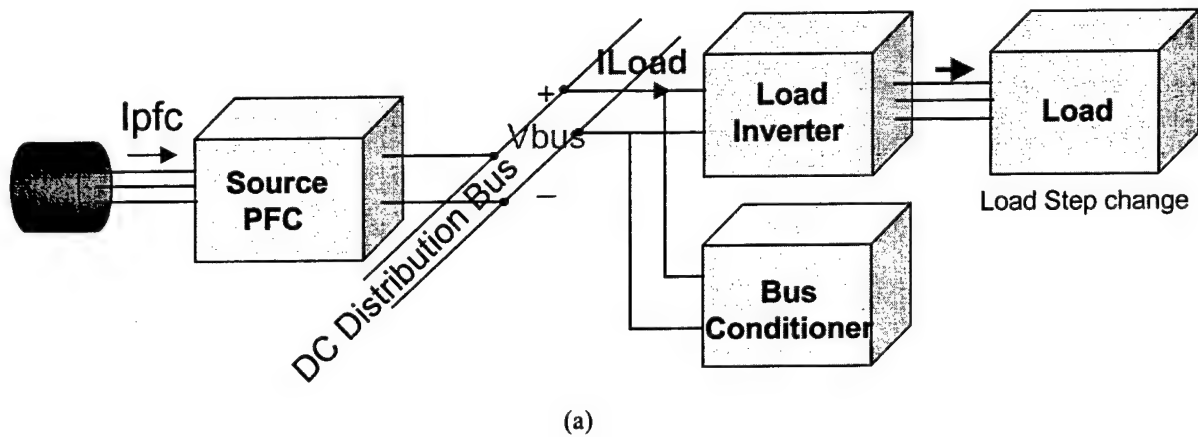
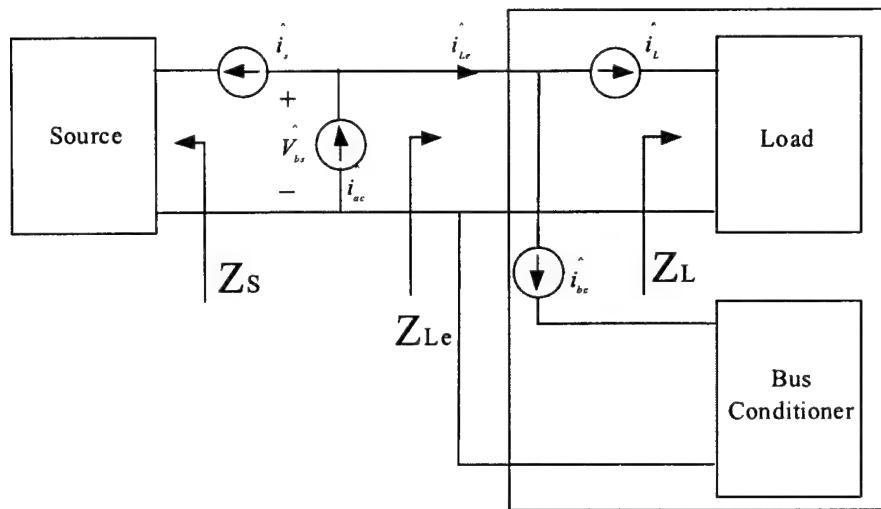
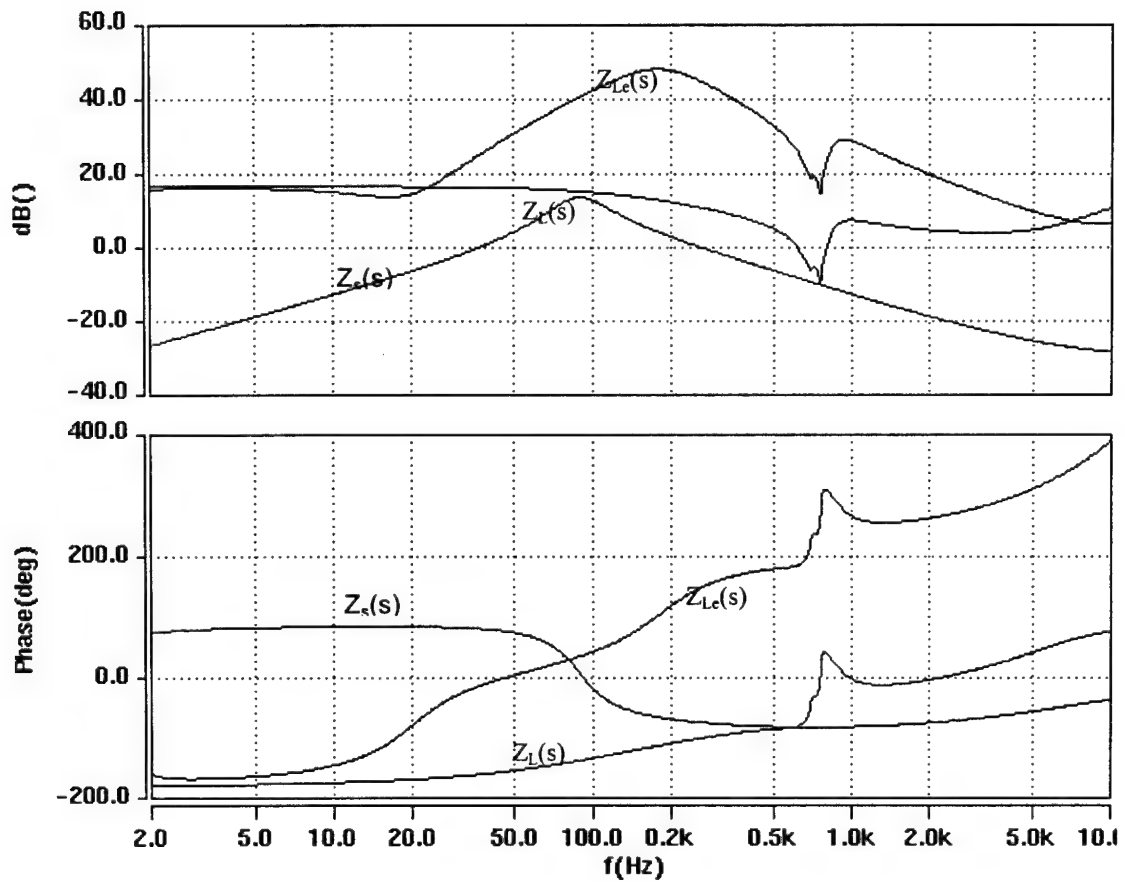


Figure 11-13. System transient performance, (a) system diagram and (b) comparison of the bus voltage.



(a)



(b)

Figure 11-14. The impedance improvement with the bus conditioner, (a) Measurement setup, (b) The comparison of the impedance.

11.4 Digital Controller Implementation of DC Bus Conditioner

The digital controller is designed to complete the control algorithm for DC bus conditioner. The digital controller consists of two main components: the DSP board and the EPLD. The controller generates PWM waveforms for the four switches of the DC bus conditioner. The relationship between the PWM waveforms of the four switches is shown in Figure 11-15.

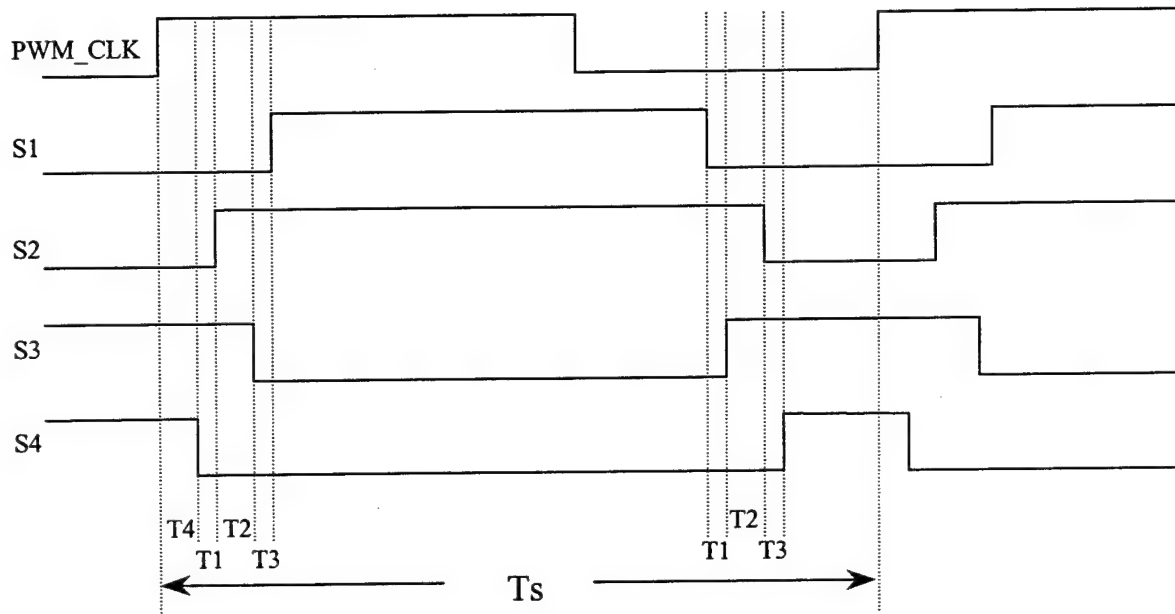


Figure 11-15. Timing chart for switches S1—S4 during a switching period.

From Figure 11-15 it can be seen that PWM signals for S1—S4 all consist of two parts: normal duty cycle and dead time. T1—T4 are designed to provide dead time among switches and, further, the voltage balance on the capacitor.

The DSP is responsible for calculating duty cycles D1—D4 and dead times T1—T4 of S1—S4. Figure 11-16 shows the flow chart of the DSP software.

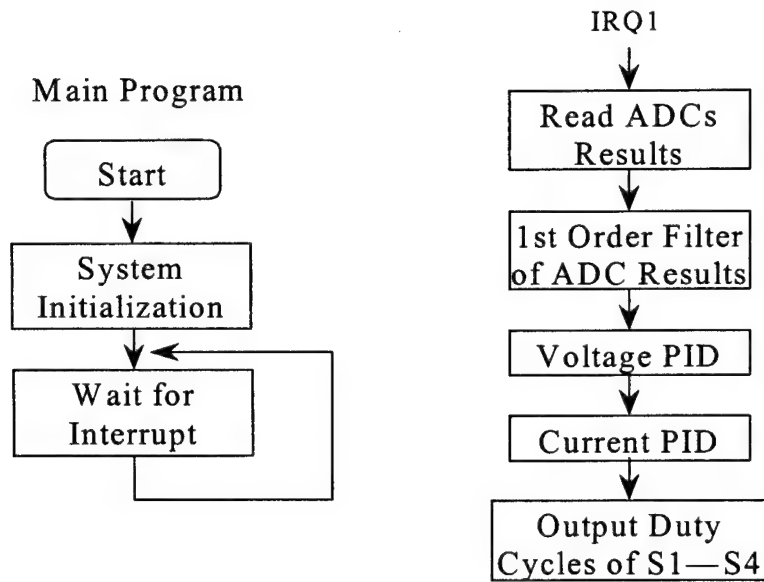


Figure 11-16. Flowcharts of DSP program.

The EPLD is responsible for generating PWM signals with correct dead time for each switch. The block diagram of the EPLD is shown in Figure 11-17.

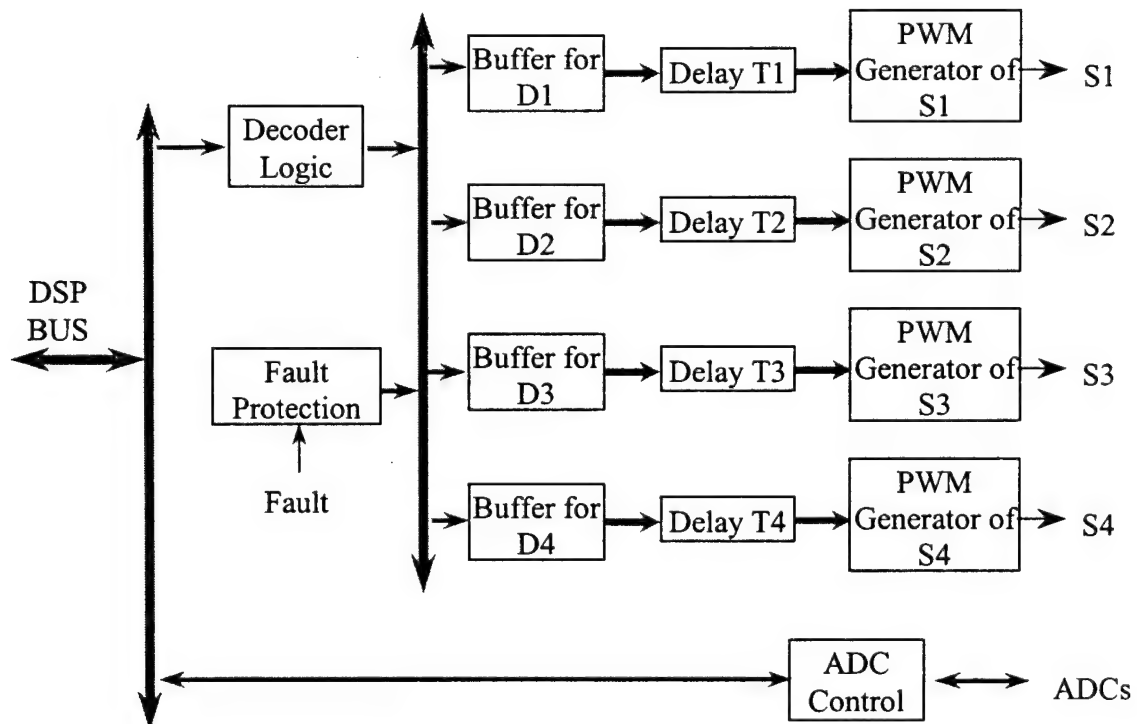
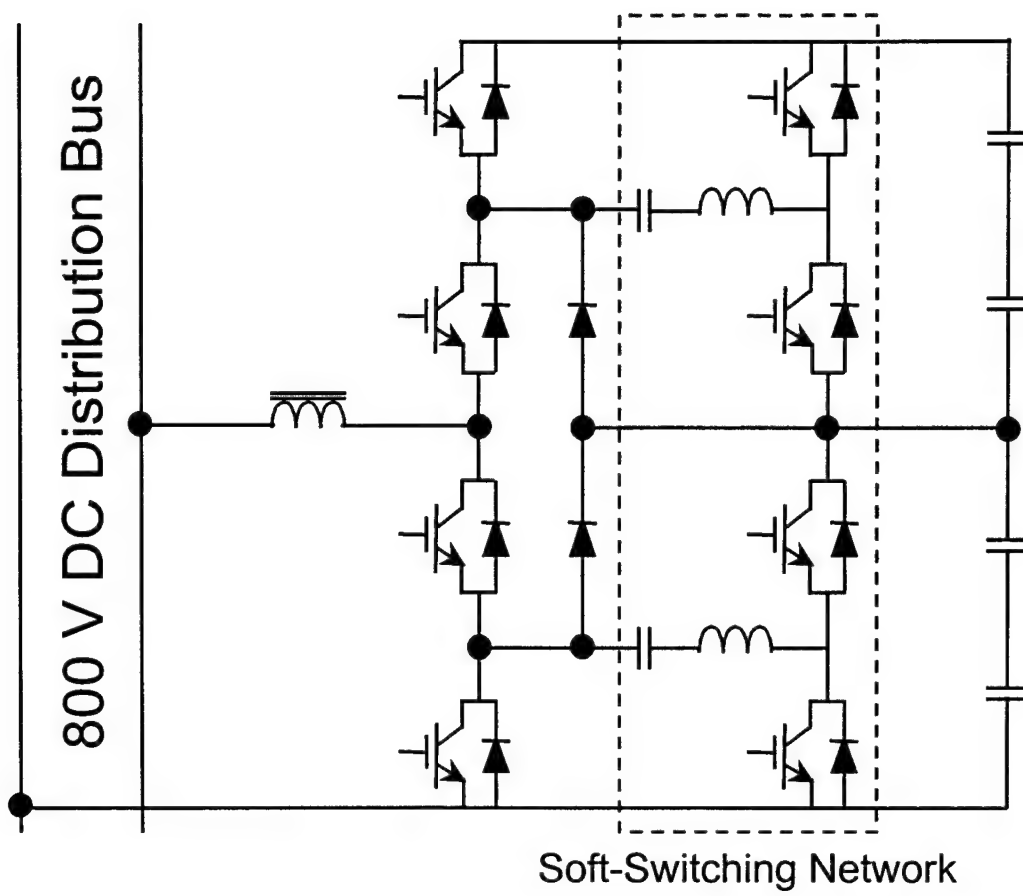


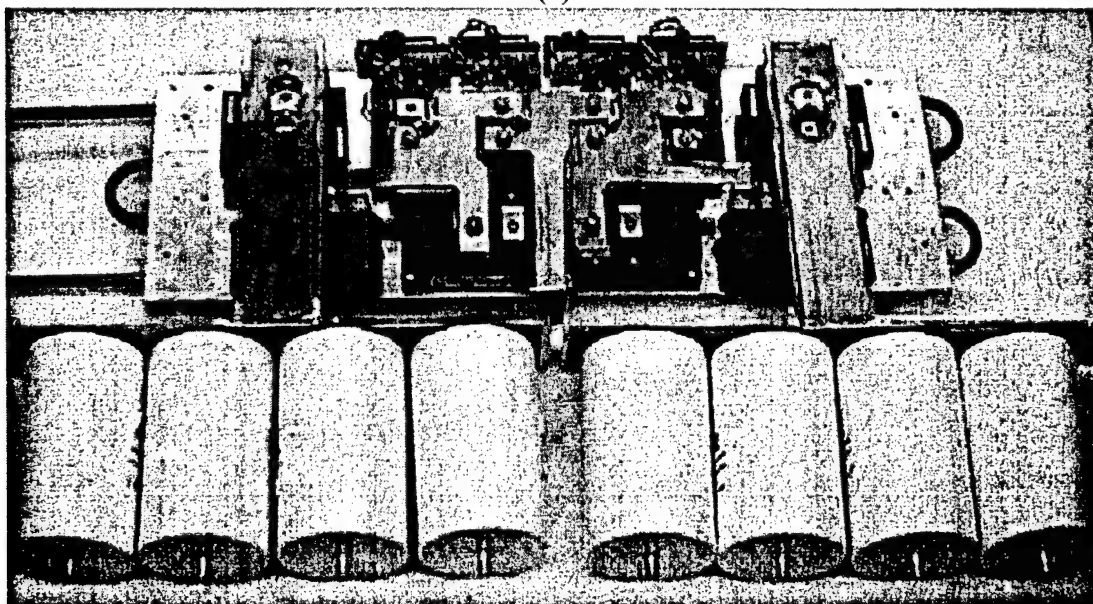
Figure 11-17. Block diagram of EPLD.

11.5 Experiments

Because the voltage of the energy storage capacitor is higher than the DC bus voltage, with a 800 V DC bus system, a three-level circuit topology is used, as shown in Figure 11-18(a). The hardware setup is shown in Figure 11-18(b). A preliminary experiment was carried out on the hardware. Figure 11-19 and Figure 11-20 show the inductor current reference signal and the produced inductor current at 120 Hz and 1 kHz. The switching frequency is 40 kHz



(a)



(b)

Figure 11-18. A three-level structure for dc bus conditioner,

(a) Circuit diagram, (b) The hardware setup

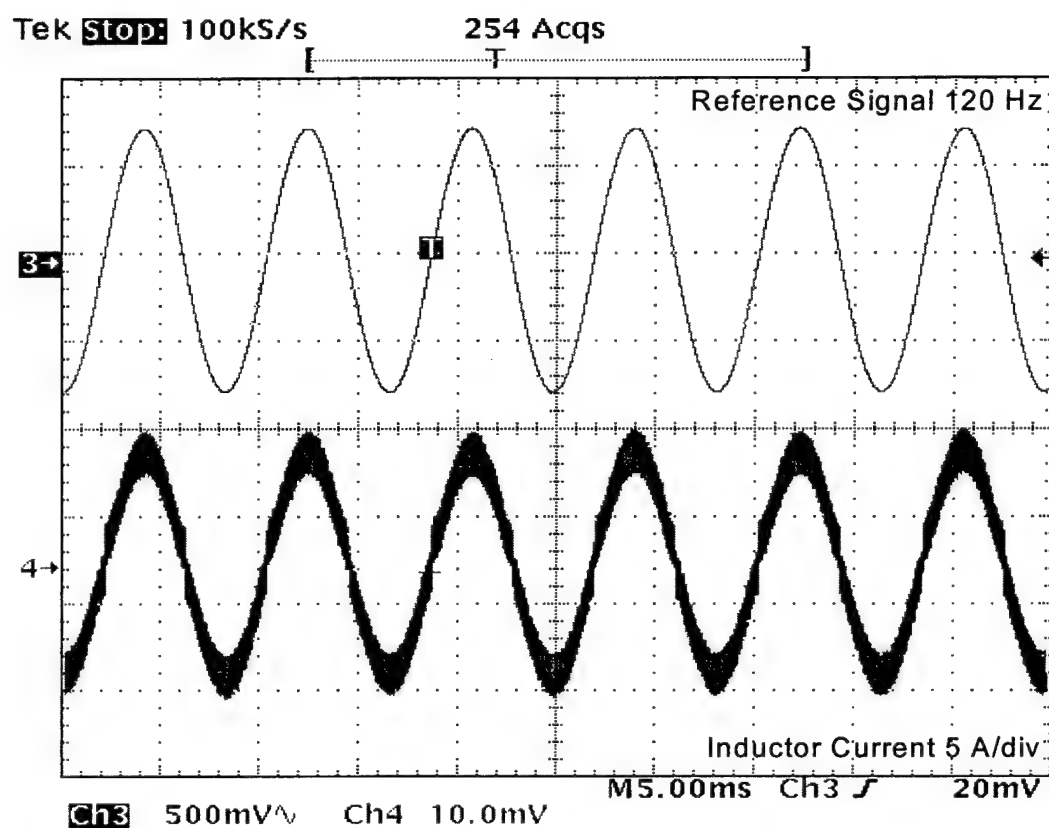


Figure 11-19. The reference signal and the inductor current at 120 Hz.

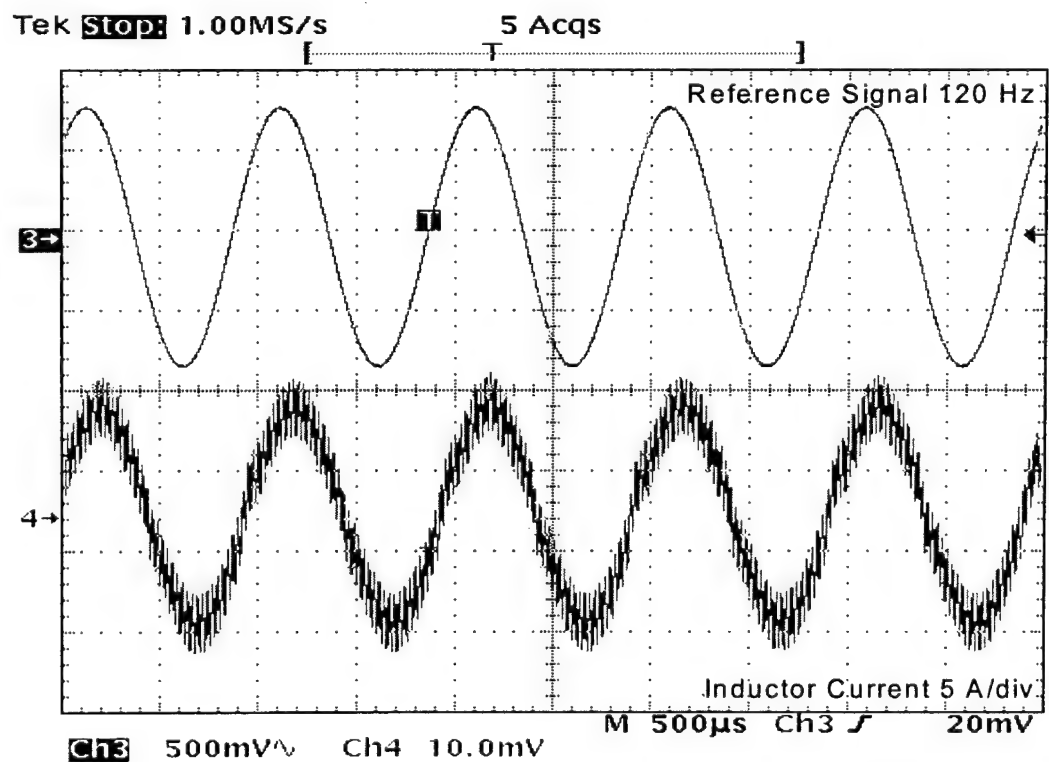


Figure 11-20 . The reference signal and the inductor current at 1 kHz.

11.6 Reference

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Chapter 12 Modeling and Control of Zero-Sequence Current

This chapter will develop an averaged model to predict the zero-sequence dynamic. Based on the developed model, a new zero-sequence current control scheme is proposed. The two-parallel, three-phase boost rectifier system in Figure 12-1 is used as an example to demonstrate the modeling and control concept, which then is generalized to any parallel multi-phase converters.

12.1 Modeling of Zero-Sequence Current

12.1.1 Phase-leg Averaging Technique

In bi-directional switch-based converters, as shown in Figure 12-1, a generic phase-leg structure, which has a voltage source on one side and a current source on the other side, can be identified.

A traditional modeling approach for a three-phase boost rectifier is to transform stationary variables into rotating coordinates. Zero-sequence components, such as zero-sequence voltage, are not reflected in the model because they do not affect control objectives, such as input line currents and output DC voltage. In order to model the zero-sequence current for the parallel rectifiers, a phase-leg averaging technique is used [8], as illustrated in Figure 12-2.

Figure 12-2 (a) shows one totem pole phase-leg of the rectifier. It has a current source in one side and a voltage source in the other. Both current and voltage are assumed continuous. Figure 12-2(b) shows the pulse-width modulation (PWM) of the switches, where d_a is defined as the duty cycle of the top switch s_{ap} , while s_{an} is the complement of s_{ap} . The corresponding voltage and current relationships are also shown in Figure 12-2(b). Based on these relationships, the averaged model of the phase-leg is depicted in Figure 12-2(c).

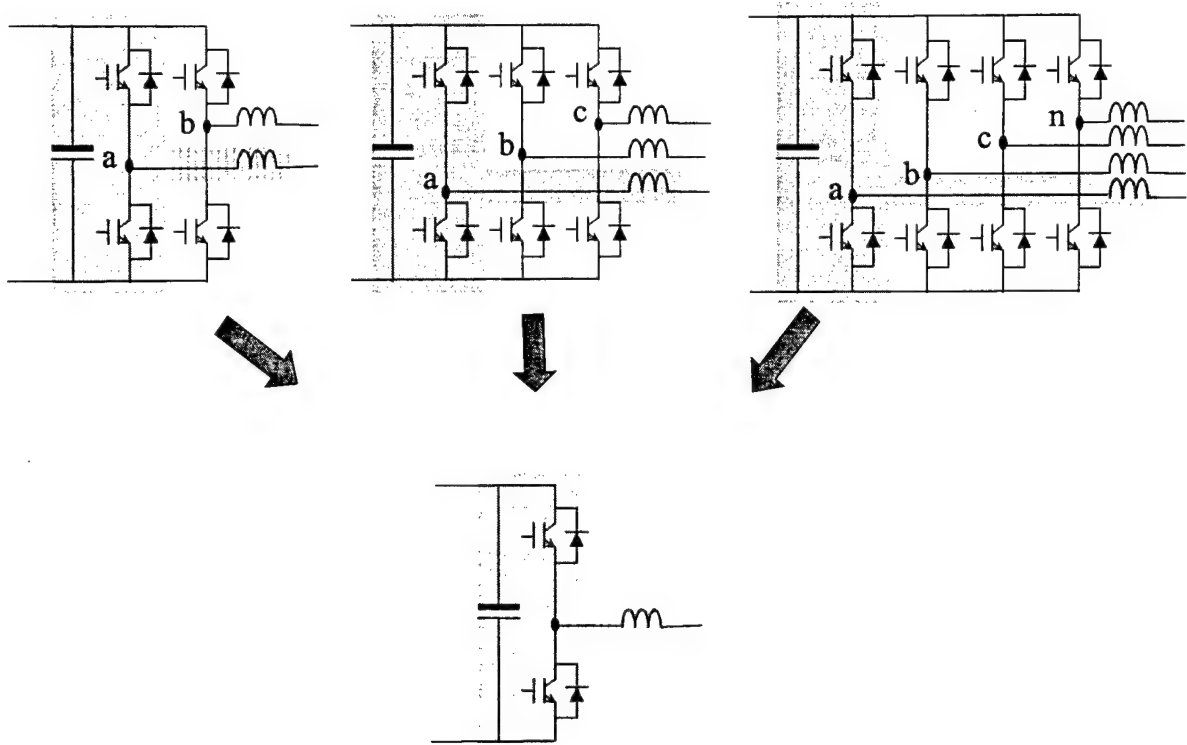
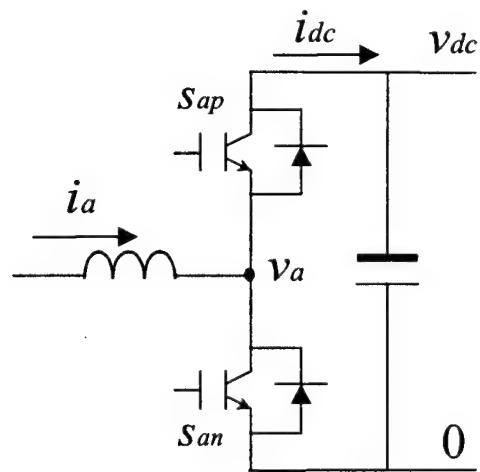
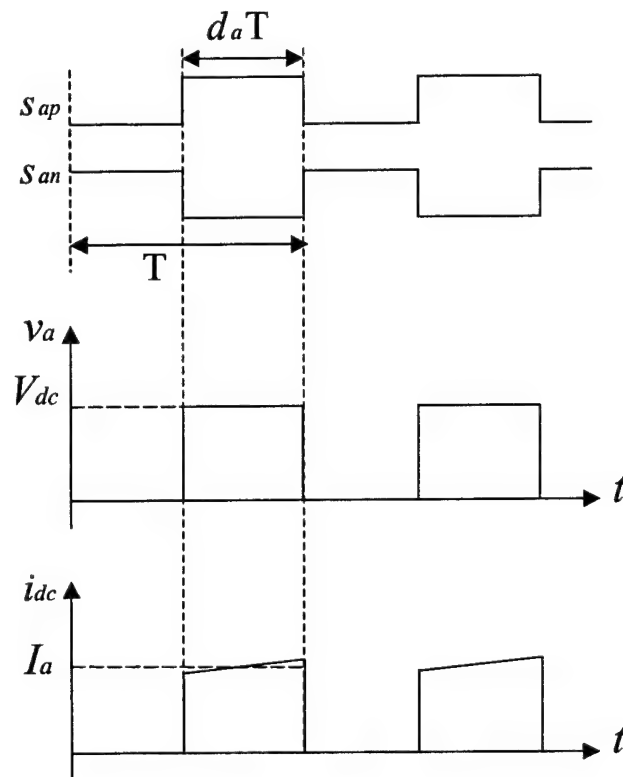


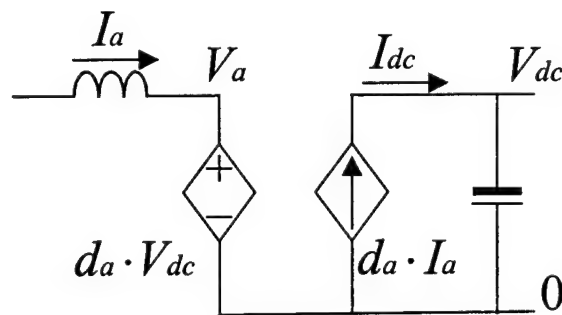
Figure 12-1. Identification of a generic phase-leg in multi-phase converters.



(a) A totem pole phase-leg cell.



(b) Switching pulses and the relationships between input and output variables.



(c) An averaged phase-leg model.

Figure 12-2. A totem pole phase-leg averaging technique.

Applying phase-leg averaging to all three legs of the rectifier, an averaged model of the rectifier is developed, as shown in Figure 12-3.

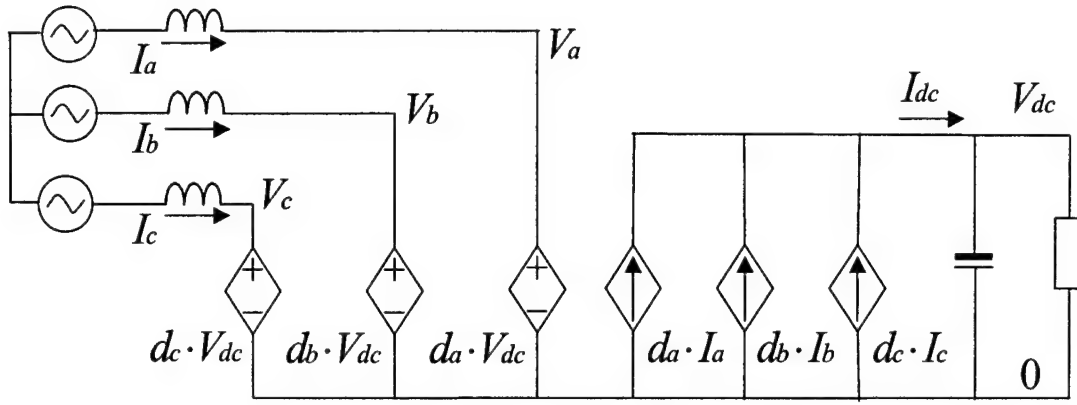


Figure 12-3. The averaged phase-leg model of a three-phase boost rectifier.

12.1.2 Extraction of Zero-sequence Components

A zero-sequence component is defined as the sum of all phase components. For example, a zero-sequence current of a three-phase boost rectifier is defined as

$$I_z = I_a + I_b + I_c . \quad (30)$$

To extract zero-sequence components, a zero-sequence duty cycle d_z is defined

$$d_z = d_a + d_b + d_c . \quad (31)$$

For a carrier-based PWM rectifier, the duty cycles d_a , d_b and d_c are sinusoidal in steady state under balanced conditions. Therefore, the sum of d_a , d_b and d_c is zero. A space-vector modulated rectifier, however, usually has triple harmonics in order to reduce switching losses, increase maximum modulation index, and improve the waveform's total harmonic distortion (THD). Therefore, the sum of the duty cycles is not equal to zero.

From (31), the following equation can be easily derived:

$$(d_a - d_z/3) + (d_b - d_z/3) + (d_c - d_z/3) = 0 . \quad (32)$$

That is

$$d_a' + d_b' + d_c' = 0 , \quad (33)$$

where d_a' , d_b' and d_c' are

$$d_a' = d_a - \frac{d_z}{3}, \quad d_b' = d_b - \frac{d_z}{3}, \quad d_c' = d_c - \frac{d_z}{3}. \quad (34)$$

Therefore, d_a , d_b and d_c can be expressed as

$$d_a = d_a' + \frac{d_z}{3}, \quad d_b = d_b' + \frac{d_z}{3}, \quad d_c = d_c' + \frac{d_z}{3}. \quad (35)$$

As a result, Figure 12-4 shows the averaged model of the three-phase rectifier with zero-sequence components. For a single rectifier, the sum of I_a , I_b and I_c has to be zero because there is no zero-sequence current path. Although a zero-sequence voltage $\frac{d_z \cdot V_{dc}}{3}$ exists in the converter, it does not affect the input currents and output voltage control.

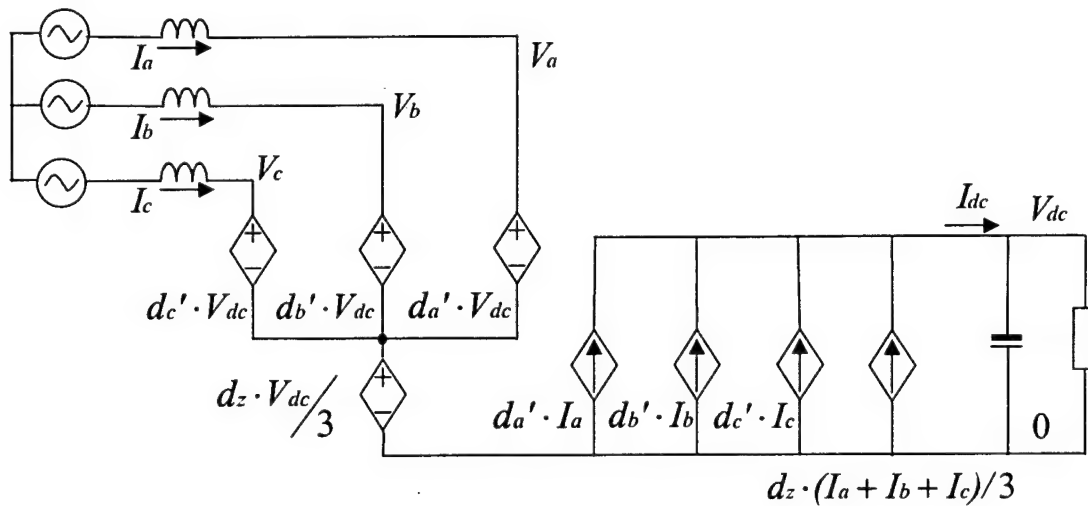


Figure 12-4. The averaged model of a three-phase PWM boost rectifier with zero-sequence components.

12.1.3 Averaged Model of Zero-sequence Dynamics

With two rectifiers in parallel, a zero-sequence current path is formed and a circulating current may occur. Figure 12-5 shows the averaged model of the two parallel three-phase rectifiers.

Summing up (37), (38) and (39), and using (33) and (36), the following equation can be derived:

$$V_{dc} \cdot (d_{z1} - d_{z2}) = (L_1 + L_2) \frac{dI_0}{dt} + (R_1 + R_2) \cdot I_0. \quad (40)$$

Equation (40) describes the dynamic of the zero-sequence components. As a result, the averaged model of the zero-sequence dynamic has been developed, and is depicted in Figure 12-6.

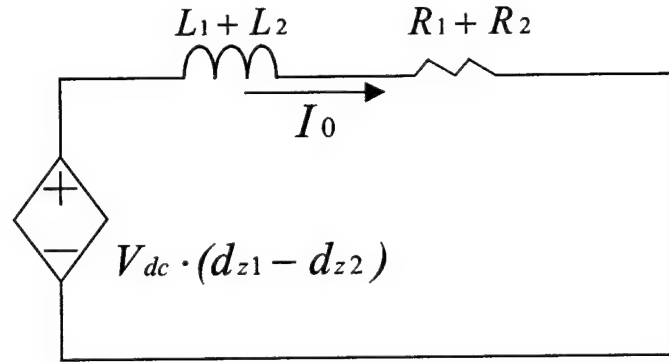


Figure 12-6. Averaged model of the zero-sequence dynamic.

12.2 Control of Zero-sequence Current

12.2.1 A New Control Variable

Different space-vector modulation (SVM) schemes produce different triple harmonics, and therefore have different duty cycles d_a , d_b and d_c . For example, Figure 12-7 shows one PWM pattern of the SVM scheme with alternate zero vectors. The d_a , d_b and d_c are the duty cycles of s_{ap} , s_{bp} and s_{cp} , respectively.

$$d_a = \frac{d_0}{2} + d_1 + d_2, \quad d_b = \frac{d_0}{2} + d_2, \quad d_c = \frac{d_0}{2}, \quad (41)$$

where d_1 and d_2 are the duty cycles of the active vectors pnn and ppn, respectively, and d_0 is the total duty cycle of the zero vectors ppp and nnn.

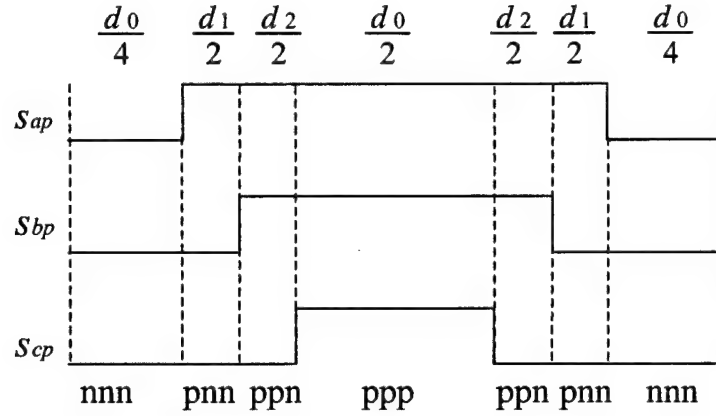


Figure 12-7. The duty cycle relationship between phase-legs and space vectors.

In this case,

$$d_z = d_a + d_b + d_c = 1.5d_0 + d_1 + 2d_2. \quad (42)$$

Although different SVM schemes have the same d_1 and d_2 in the synthesis of a reference vector, d_z can differ. The distribution of the zero vectors can vary without affecting the control objectives, such as the input AC currents and the output DC voltage. This indicates that d_z can be controlled by the distribution of d_0 . Based on this idea, a new control variable k is introduced as follows:

$$k = \frac{d_{ppp}}{d_0}, \quad (43)$$

where d_{ppp} is the time period for applying the zero vector ppp, as illustrated in Figure 12-8.

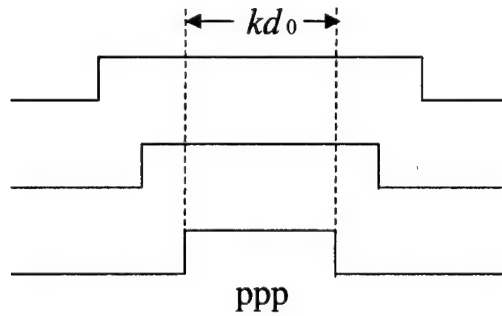


Figure 12-8. The definition of the new control variable k .

Usually, for the scheme with alternate zero vectors, $k=0.5$, as shown in Figure 12-8. With the definition in (43), (42) can be rewritten as

$$d_z = d_a + d_b + d_c = 3kd_0 + d_1 + 2d_2. \quad (44)$$

Then, the difference of d_z of the two rectifiers is expressed as

$$d_{z1} - d_{z2} = 3d_0(k_1 - k_2). \quad (45)$$

As a result, the new averaged model of the zero-sequence dynamic with the new control variable k is shown in Figure 12-9.

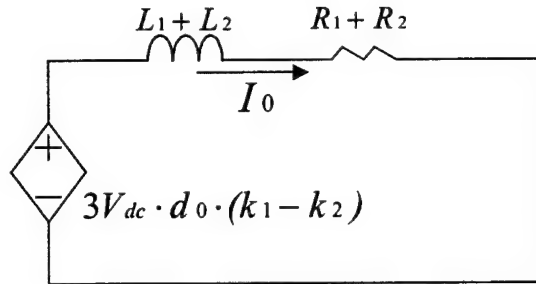


Figure 12-9. Averaged zero-sequence model with the new control variable k .

12.2.2 Implementation of Zero-Sequence Current Control

Since it is a first-order system, the control bandwidth of the zero-sequence current loop can be designed to be very high, and a strong current loop that suppresses the zero-sequence current can be achieved.

One rectifier needs only two current sensors to implement power factor correction, because the sum of the three line currents is always zero. With two rectifiers in parallel, three current sensors are needed in order to obtain the zero-sequence current. Figure 12-10 shows the implementation of the zero-sequence current control. In a two-parallel converter system, it is sufficient to control one of the two converters since there is only one zero-sequence current. The shaded block is the zero-sequence current controller added onto the other control parts of the rectifier.

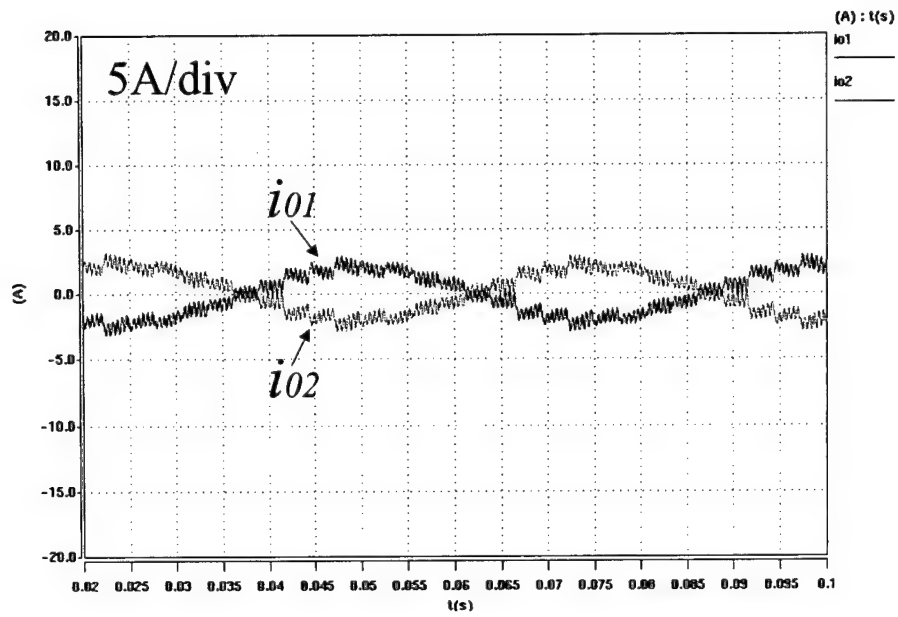
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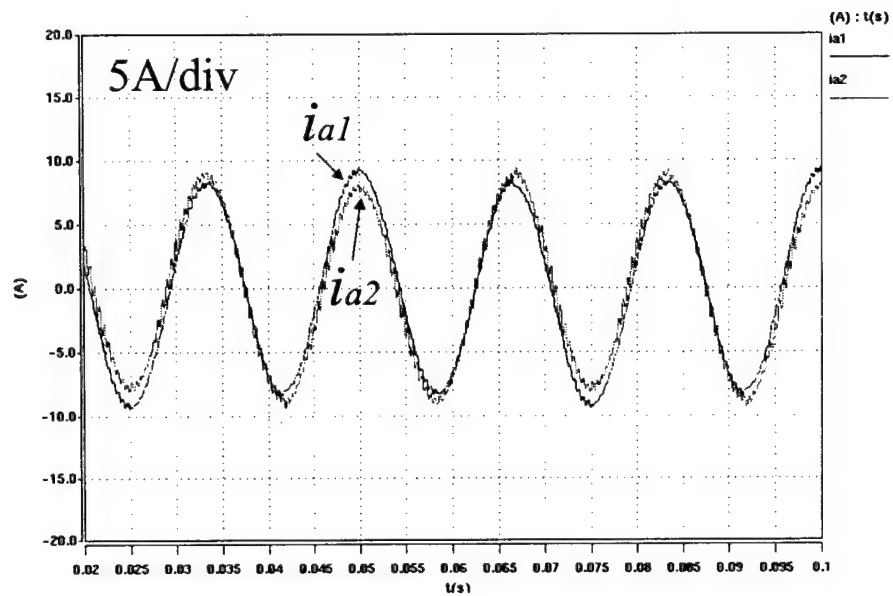
12.3 Simulation and Experimental Results

The simulation model was developed using SABER. Without the zero-sequence current control, any discrepancies between the two rectifiers (different switching frequencies, different power stage parameters or different switching deadtime, for example, each of which was demonstrated in simulation) may cause a large circulating current. Figure 12-11 shows two rectifiers with switching frequencies of 32 kHz and 16 kHz. Figure 12-11(a) shows that a significant low-frequency circulating current exists in the system. The i_{o1} and i_{o2} are zero-sequence currents for rectifiers 1 and 2, respectively. The circulating current causes distorted input line currents i_{a1} and i_{a2} , as shown in Figure 12-11(b). By applying the zero-sequence current control, the waveforms in Figure 12-12 show that the circulating current is almost gone. Only high-frequency current ripples still exist, and they can be easily attenuated.

The experimental results are shown in Figure 12-13 and Fig. 30. A two-parallel, three-phase boost rectifier breadboard system was built and tested. Figure 12-13 shows the zero-sequence currents and the line currents without zero-sequence current control, whereas Figure 12-14 shows the waveforms with control. Due to non-uniform practical conditions, such as different delays of clock signals, the experimental waveforms are less uniform than simulation waveforms. Also, three noticeable ripples in Figure 12-14(a) are due to distortion introduced by zero-crossing detection.

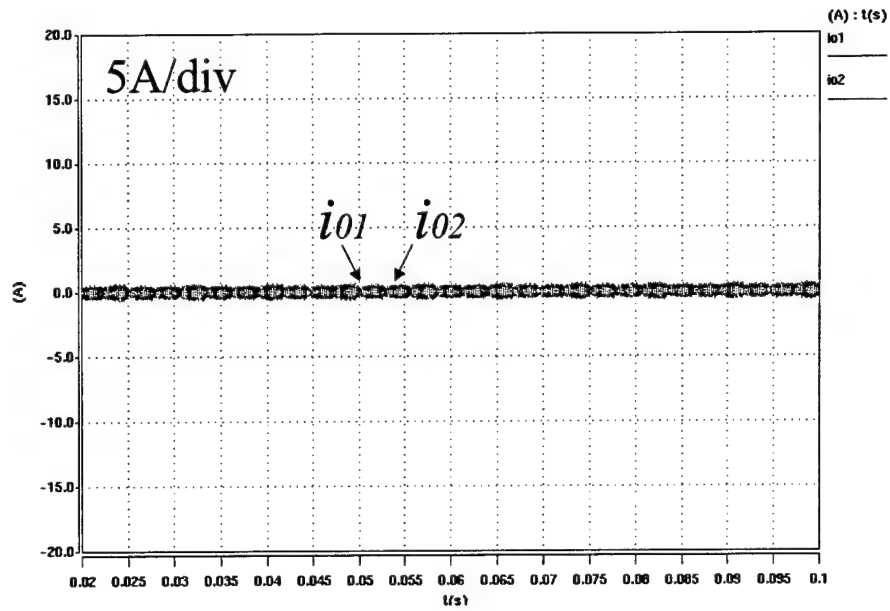


(a) The zero-sequence currents.

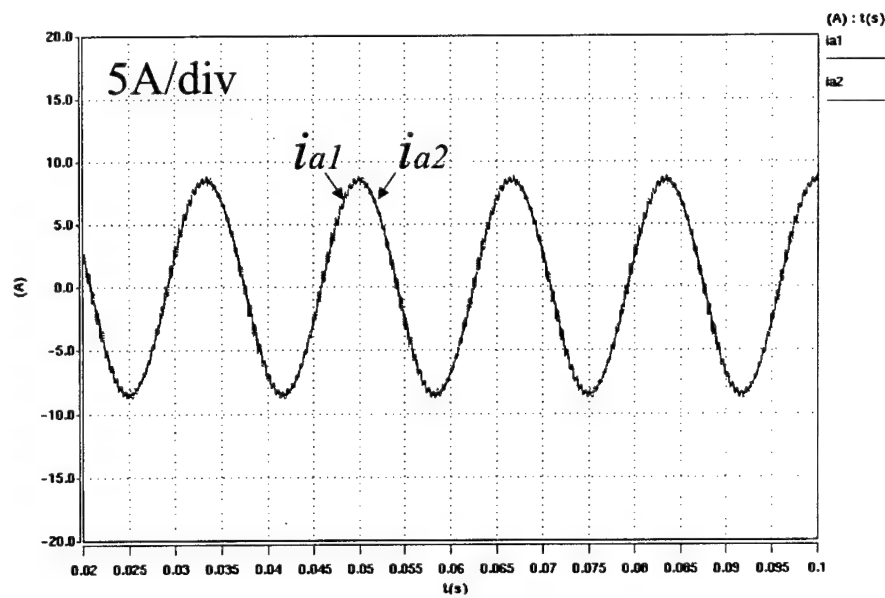


(b) The input phase currents.

Figure 12-11. Simulated waveforms without zero-sequence current control
(fsw1=32 kHz, fsw2=16 kHz).

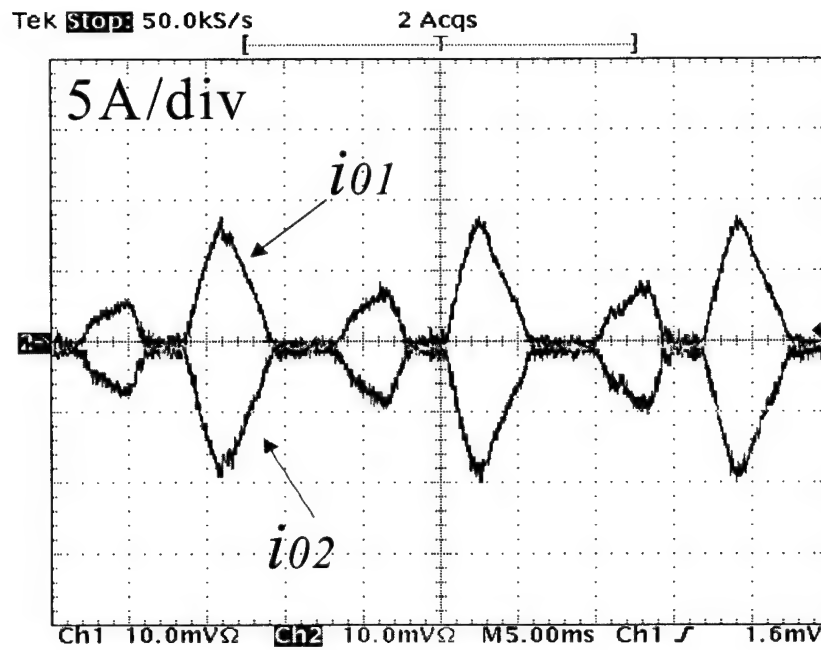


(a) The zero-sequence currents.

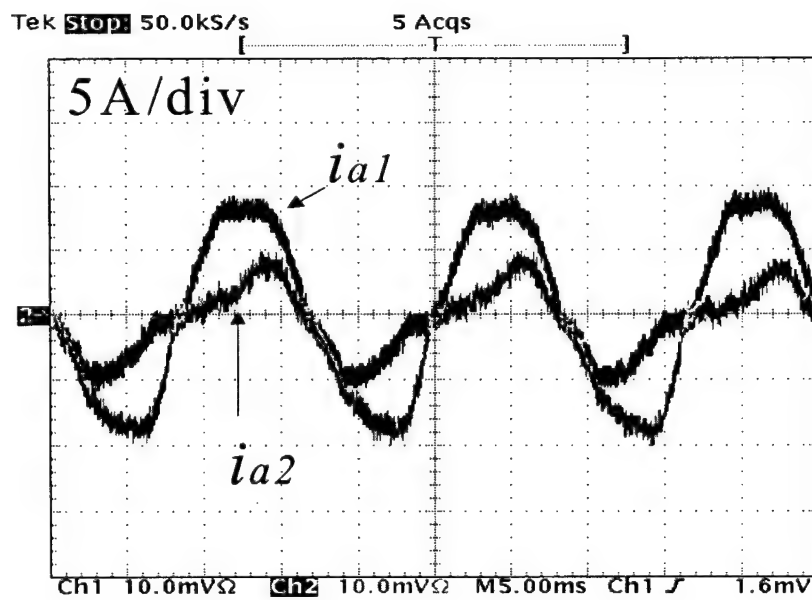


(b) The input phase currents.

Figure 12-12. Simulated waveforms with zero-sequence current control
(fsw1=32 kHz, fsw2=16 kHz).

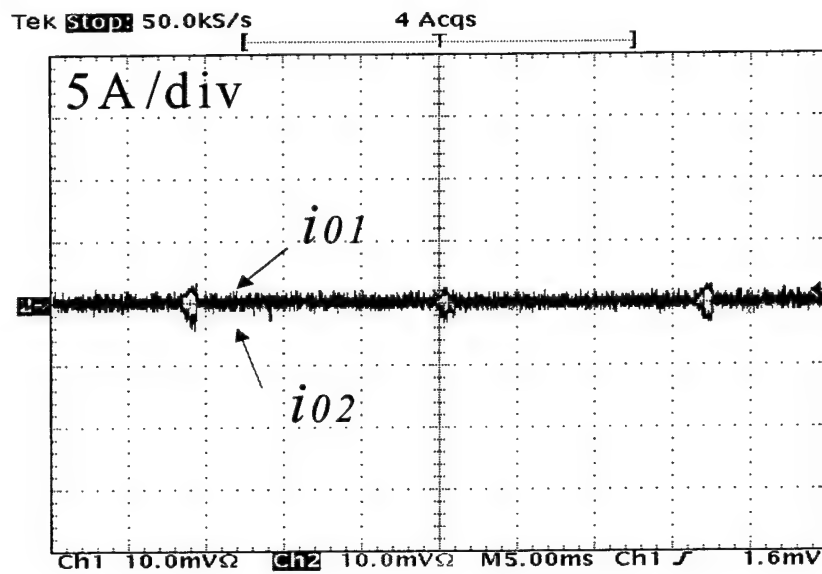


(a) The zero-sequence currents.

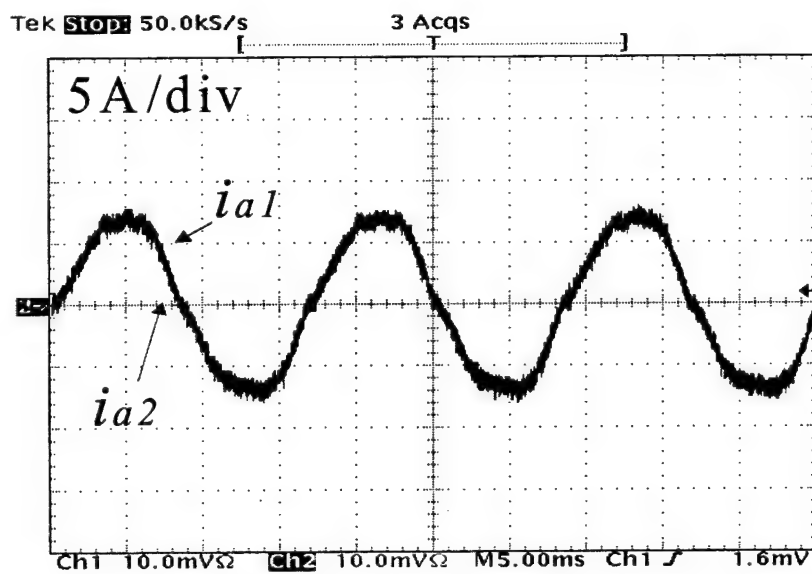


(b) The input phase currents.

Figure 12-13. Experimental waveforms without zero-sequence current control (fsw1=32 kHz, fsw2=16 kHz, unsynchronized).



(a) The zero-sequence currents.



(b) The input phase currents.

Figure 12-14. Experimental waveforms with zero-sequence current control
(fsw1=32 kHz, fsw2=16 kHz, unsynchronized).

12.4 Generalization of Zero-Sequence Modeling and Control Concept

Figure 12-15 shows an averaged phase-leg model of a general multi-phase converter. Referring to Figure 12-1, for a full-bridge converter, $m=2$ and $m_{1,2}=a,b$; for a three-phase, three-leg converter, $m=3$ and $m_{1,2,3}=a,b,c$; and for a three-phase, four-leg converter, $m=4$ and $m_{1,2,3,4}=a,b,c,n$. A zero-sequence duty-cycle is defined as

$$d_z = d_{m1} + \dots + d_{mm} . \quad (46)$$

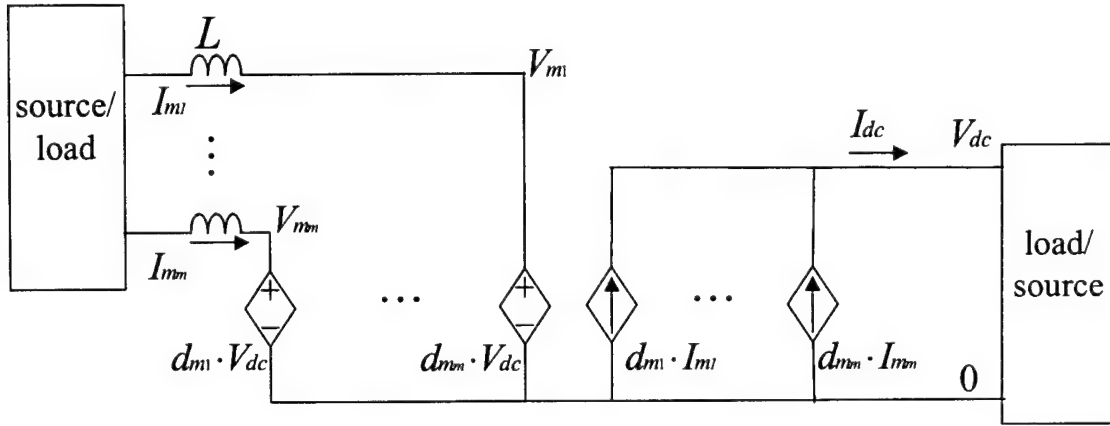


Figure 12-15. A generalized averaged model of a multi-phase converter.

From the definitions:

$$d_{m1}' = d_{m1} - \frac{d_z}{m} , \dots , d_{mm}' = d_{mm} - \frac{d_z}{m} . \quad (47)$$

the following equation can be easily derived

$$d_{m1}' + \dots + d_{mm}' = 0 . \quad (48)$$

Then d_{m1}, \dots, d_{mm} can be expressed as follows:

$$d_{m1} = d_{m1}' + \frac{d_z}{m} , \dots , d_{mm} = d_{mm}' + \frac{d_z}{m} . \quad (49)$$

As a result, one can obtain the averaged model of the multi-phase converter with zero-sequence components, as shown in Figure 12-16.

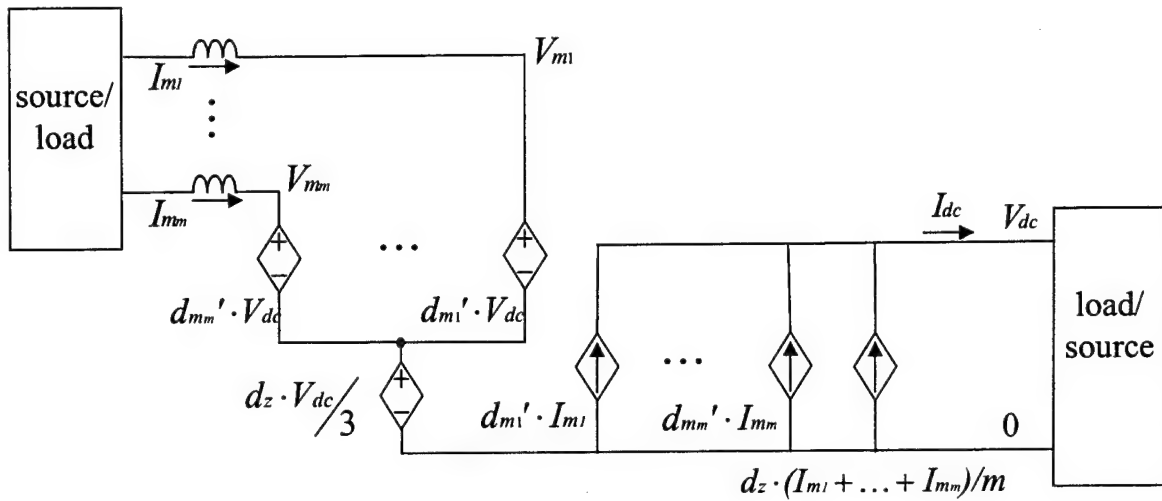


Figure 12-16. The averaged model of the multi-phase converter with zero-sequence components.

With two multi-phase converters in parallel, as shown in Figure 12-17, a zero-sequence current path is formed. The zero-sequence current is defined as the sum of all phase currents with the direction defined in Figure 12-17.

$$I_0 = I_{01} = I_{m11} + \dots + I_{mm1} = -I_{02} = -(I_{m12} + \dots + I_{mm2}) \quad (50)$$

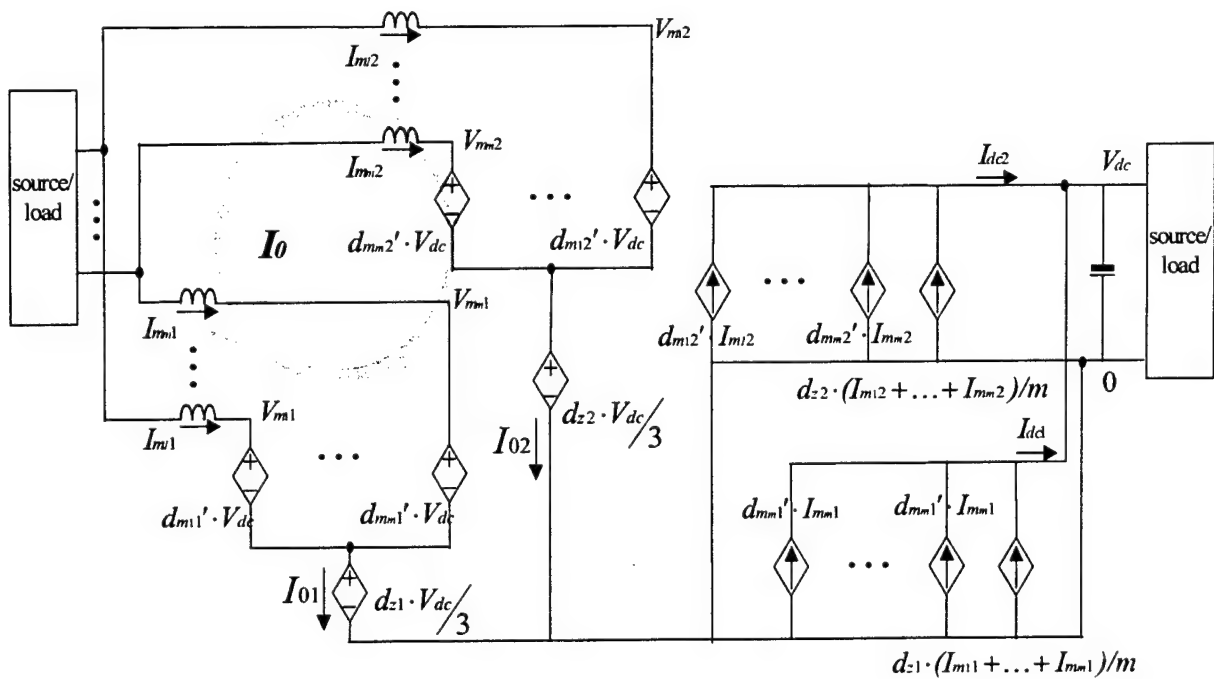


Figure 12-17. An averaged model of a parallel multi-phase converter system.

In the AC side of Figure 12-17, there are m loops forming m equations as follows:

$$d_{z1} \cdot V_{dc}/3 + d_{m11}' \cdot V_{dc} - L_1 \frac{dI_{m11}}{dt} - R_1 \cdot I_{m11} = d_{z2} \cdot V_{dc}/3 + d_{m12}' \cdot V_{dc} - L_2 \frac{dI_{m12}}{dt} - R_2 \cdot I_{m12}, \quad (51)$$

... .. ,

$$d_{z1} \cdot V_{dc}/3 + d_{mm1}' \cdot V_{dc} - L_1 \frac{dI_{mm1}}{dt} - R_1 \cdot I_{mm1} = d_{z2} \cdot V_{dc}/3 + d_{mm2}' \cdot V_{dc} - L_2 \frac{dI_{mm2}}{dt} - R_2 \cdot I_{mm2}, \quad (52)$$

where R_1 and R_2 are ESRs of the inductor L_1 and L_2 , respectively. Summing up (51) to (52), and using (48) and (50), one can obtain

$$V_{dc} \cdot (d_{z1} - d_{z2}) = (L_1 + L_2) \frac{dI_0}{dt} + (R_1 + R_2) \cdot I_0. \quad (53)$$

Equation (53) describes the dynamic of the zero-sequence current. Figure 12-18 shows the equivalent circuit of equation (53). It can be seen that the equivalent circuit is exactly the same as the one in Figure 12-6, meaning that any parallel multi-phase converters have the same format of zero-sequence dynamics.

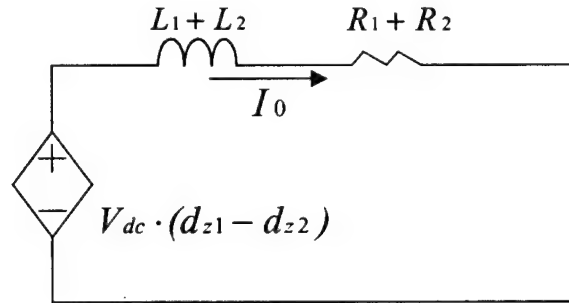


Figure 12-18. An averaged model of zero-sequence current dynamic.

To control the zero-sequence current, a new control variable associated with the PWM is introduced. The new control variable k is defined as the duration when all top switches are on (p-state):

$$k = dp_{m1} \dots p_{mm}. \quad (54)$$

Figure 12-19 depicts the k in one switching pattern of a multi-phase converter. As an example, k is the duration of zero-vector ppp in a three-phase, three-leg converter. Usually, for a scheme with alternate zero vectors, $k=0.5d_0$. With this definition in (46) and (54),

$$d_z = d_{m1} + \dots + d_{mm} = mk + \sum d_{active}, \quad (55)$$

where d_{active} is the duty cycle of active vectors. The PWM of a multi-phase converter has fixed duty cycles of active vectors at certain reference points, while the choice of zero vectors is flexible in a single converter operation. Switching losses and waveform THDs are usually the considerations in choosing a zero vector pattern.

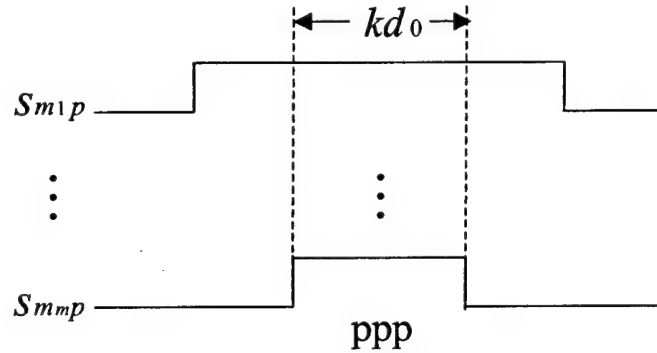


Figure 12-19. The definition of the control variable k .

The idea of the proposed zero-sequence current control scheme is to control the k , i.e. the distribution of zero vectors. By replacing d_z in (53) with (55), it becomes:

$$mV_{dc} \cdot (k_1 - k_2) = (L_1 + L_2) \frac{dI_0}{dt} + (R_1 + R_2) \cdot I_0. \quad (56)$$

Equation (56) illustrates that the zero-sequence current can be controlled by controlling k . Since the dynamic of (56) is a first-order system, the control bandwidth can be designed to be very high. Figure 12-20 shows the zero-sequence current controller for the parallel multi-phase converters.

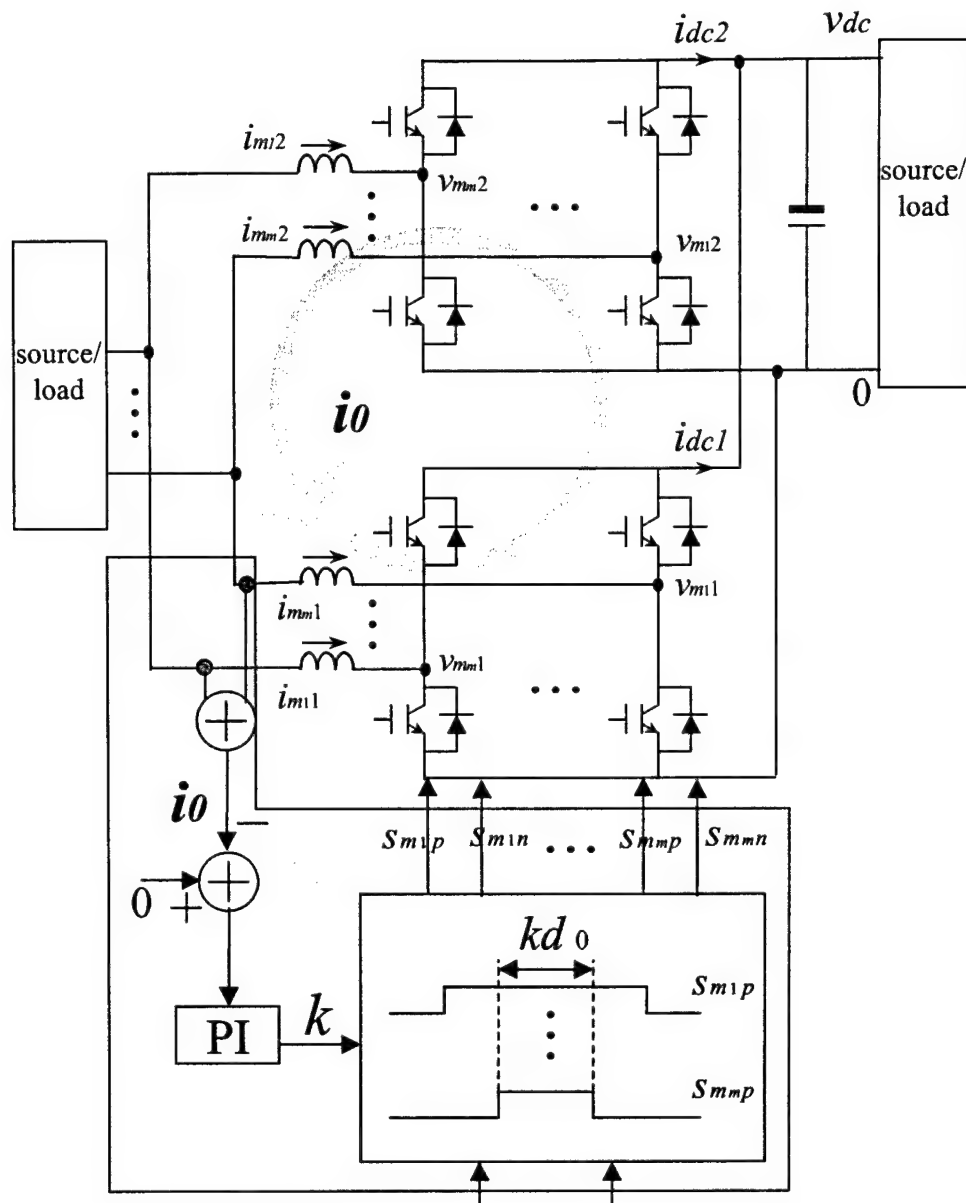


Figure 12-20. A zero-sequence current controller for a multi-phase converter.

In a two-parallel converter system, it is sufficient to control one of the two converters since there is only one zero-sequence current. For an n -parallel converter system, there are $n-1$ independent zero-sequence currents. Therefore, $n-1$ converters need to have a zero-sequence current controller.

12.5 High-Frequency Noise Reduction

In order to cancel high-frequency common-mode dv/dt , a symmetrical circuit structure is required. Normally, a single multi-phase converter does not provide the symmetrical structure. However, a parallel converter system naturally provides this structure.

Figure 12-21 shows a parallel inverter system that uses the midpoint of the DC input as a reference point.

The circuit has equations:

$$v_{a1} = L \frac{di_{a1}}{dt} + Zi_a + v_n, \quad v_{b1} = L \frac{di_{b1}}{dt} + Zi_b + v_n, \quad v_{c1} = L \frac{di_{c1}}{dt} + Zi_c + v_n \quad \text{and} \quad (58)$$

$$v_{a2} = L \frac{di_{a2}}{dt} + Zi_a + v_n, \quad v_{b2} = L \frac{di_{b2}}{dt} + Zi_b + v_n, \quad v_{c2} = L \frac{di_{c2}}{dt} + Zi_c + v_n. \quad (59)$$

Summing up (58) and (59), the following equation can be obtained

$$\begin{aligned} v_{a1} + v_{b1} + v_{c1} + v_{a2} + v_{b2} + v_{c2} = \\ L \frac{d(i_{a1} + i_{b1} + i_{c1} + i_{a2} + i_{b2} + i_{c2})}{dt} + 2Z(i_a + i_b + i_c) + 6v_n. \end{aligned} \quad (60)$$

Since

$$i_{a1} + i_{b1} + i_{c1} + i_{a2} + i_{b2} + i_{c2} = 0, \quad \text{and} \quad (61)$$

$$i_a + i_b + i_c = 0, \quad (62)$$

the common-mode voltage v_n is described as:

$$v_n = \frac{v_{a1} + v_{b1} + v_{c1} + v_{a2} + v_{b2} + v_{c2}}{6}. \quad (63)$$

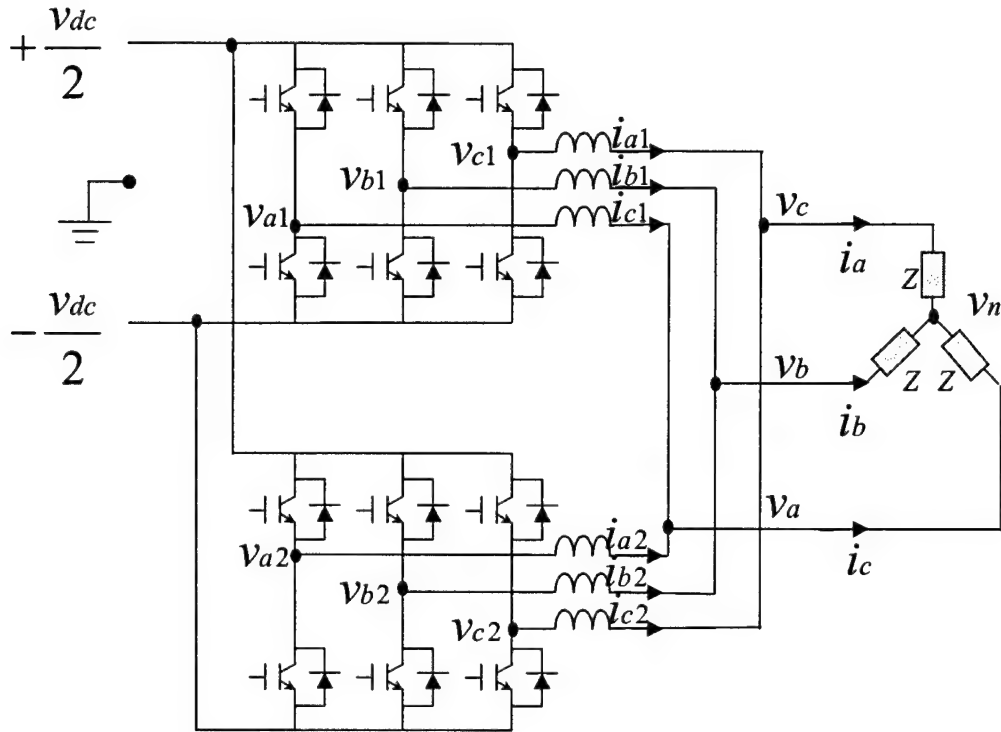


Figure 12-21. A parallel inverter system.

Compared with that of a single inverter in (57), the parallel inverters are able to reduce the common-mode voltage V_n by canceling out among bridge voltages V_{a1} , V_{b1} , V_{c1} , V_{a2} , V_{b2} and V_{c2} .

The condition for common-mode cancellation is

$$V_{a1} + V_{b1} + V_{c1} + V_{a2} + V_{b2} + V_{c2} = 0. \quad (64)$$

This work proposes a modulation scheme, in which the two converters use a symmetrical SVM with opposite zero vectors, as shown in Figure 12-22. The resulting common-mode voltage is significantly reduced. This scheme results in fewer voltage jumps with lower magnitude.

Meanwhile, this is an interleaving scheme, so the differential-mode ripple can be reduced as well. Figure 12-23 shows the differential-mode ripple reduction.

In conclusion, the parallel converter system with synchronization and interleaving can reduce both the differential-mode ripple and the common-mode dv/dt noise. These reductions make the parallel structure more attractive.

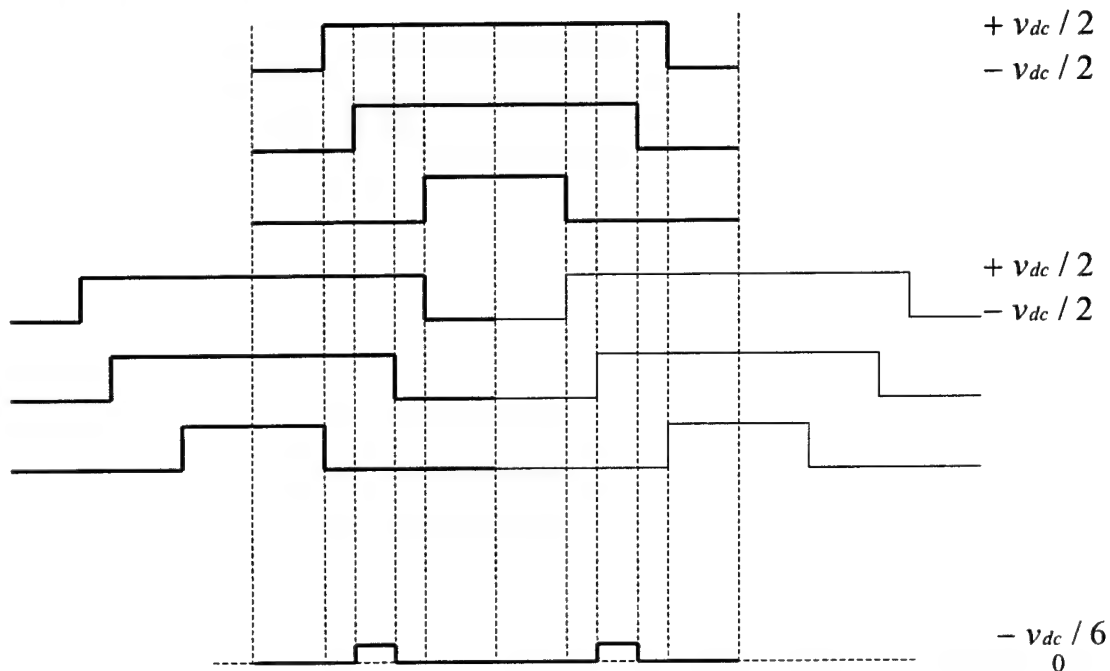


Figure 12-22. A proposed PWM for the parallel converter system to reduce the differential-mode ripple and the common-mode noise.

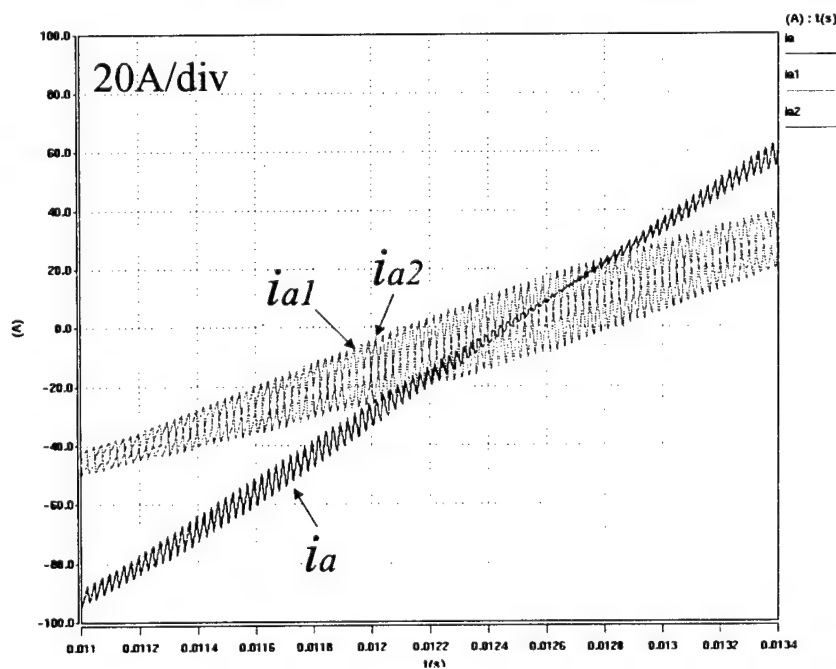


Figure 12-23. Interleaved waveforms of the inductor currents.

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Chapter 13 Modularized Control Architecture

13.1 INTRODUCTION

The need for low-cost, high-reliability, easy-to-use power processing devices is becoming more and more pronounced [1]. Long design cycles, complex maintenance, a lack of standardization and high cost are slowing down possibilities for wider proliferation of power converters.

Power electronics has reached the point where further advancement, in terms of wider application of converters can hardly be achieved unless the community is presented with easy to use, of-the-shelf, reliable and flexible power electronics modules [1], [2], [3]. These modules may not be optimal from the cost point of view, but they would solve the problem of long design cycles and low reliability. Having flexible and multifunctional power processing units that cover a wide range of applications would provide higher production volume, thus reducing manufacturing costs. Furthermore, it would enable power electronics solutions for a large number of specific applications that can not justify single application development costs.

In order to fulfill these requirements, future power electronics converters should have several predominant features, such as:

- a high level of integration, to improve reliability and lower costs;
- flexibility, to provide the necessary level of system adaptability and multifunctionality;
- in-circuit programmability, to allow for simple software and hardware reconfiguration and use of one standardized module in different applications; and
- user-friendliness, to enable the wider engineering community to create their own applications, thus focusing engineering efforts towards system-oriented design.

What is needed to bring the whole concept to its full potential is a general solution for the controller that will be able to support all necessary functions. The widely used concept,

relying on a centralized digital controller [5] has several major drawbacks [8], thus indicating the need for a different approach in controller design and implementation.

This paper therefore presents a new approach to the problem, which utilizes the idea of a distributed controller, well-suited for medium and high-power converters and which is in full compliance with above-mentioned design guidelines.

The concept of a distributed controller has been explored in motion control systems [9], from which we initially borrowed the idea. The novelty of this approach is in the fact that we are designing a distributed controller on a power converter level, compared with a motion control network in which motor and controller are treated as one smart actuator. This difference introduces new control and communication issues.

Some work has already been done regarding the control and communication issues where a distributed controller has been implemented at the converter level. Malapelle et al. [7] proposed a distributed digital control for high-power drives, splitting the controller on a regulator (dedicated to motor control), and a bridge controller (providing necessary firing signals for bridge switches) connected with a relatively slow parallel bus. Toit et al. [6] have proposed a more advanced distributed control structure, where each phase leg is controlled by a separate controller. Vital data for operation of the system is being communicated between the controller and phase legs through the daisy-chained fiber optical link (2.5 Mbits/sec), while the current (and/or voltage) loop is being closed locally through the phase leg Digital Signal Processor (DSP).

The distributed controller discussed in this paper proposes a new control partitioning that falls along the natural boundary of technical expertise. Control engineers focus on the application and system issues, not the actual power hardware control. While power electronic engineers focus on the power conversion hardware and not the application. The proposed architecture consists of an application manager and one or more hardware managers linked with a high speed (125Mbits/sec) fiber-optical daisy-chained network. The application manager, liberated from any hardware-oriented tasks becomes a universal and converter independent entity. While the hardware manager, designed as an

integral part of the power stage, handles hardware-specific tasks and provides a high level of module adaptability.

13.2 CONCEPT OF DISTRIBUTED DIGITAL CONTROLLER

For an effective design that would have inherent reusability an object oriented hardware design strategy was adopted. Additionally, the technology that was to be exploited should lend itself to affordability. Consider a set of widely used power electronics converters given in Figure 13-1. Partitioning them, on a phase-leg basis, a universal power converter building block cell can readily be identified. With this common switching cell, families of different switching power converters such as AC/DC, DC/AC, DC/DC and AC/AC can be constructed. Furthermore, modularization of the control structure consistent with this common building block identifies a need for an intelligent building block and an application level controller. The concept of a smart, universal, modular and flexible power conversion building block can be realized by integrating the common switching cell, the gate drivers, sensors and some local intelligence. These two basic blocks (application controller and intelligent switching module) with a proper interface could cleanly be partitioned. This interface becomes the power of the design.

In general, universal interfaces can be designed with either a parallel or serial bus. A parallel bus is expensive, bulky and EMI-prone. By selecting a high-bandwidth serial communication interface, sensor feedback signals could be routed via digital communication simplifying interconnections and extending system flexibility. This also leverages emerging communication technology, which is expected to eventually lower cost.

Within the integrated power module, the embedded control architecture, together with gate drives, sensors, and communication interface is defined as the hardware manager. Consequently, the power building block consists of a common switching cell and its associated hardware manager.

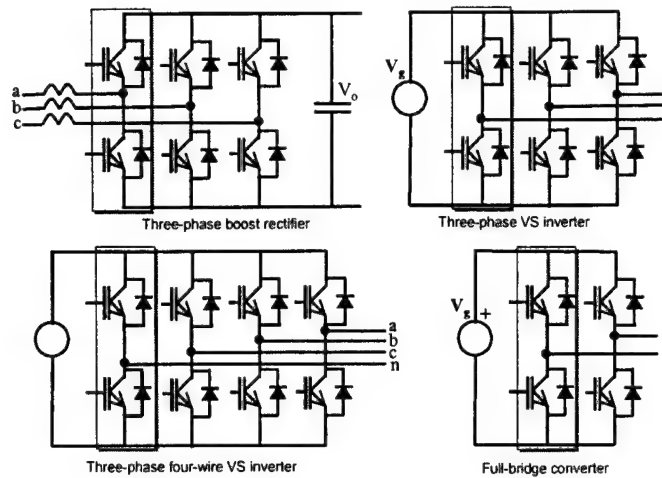


Figure 13-1. Common converter topologies.

By splitting the controller between power processing units and the main controller (Figure 13-2.), defined as the application manager, a new component the communication link (interface I_1 in Figure 13-2) is being introduced in to the control architecture. By means of open, flexible and high-bandwidth communication link the system will gain additional level of flexibility and adaptability.

Finally, a new distributed control architecture comprising three main components- application manager, hardware manager and communication link, shown in Figure 13-2. can be established. One of the typical examples, the three-phase voltage source inverter (VSI), has been built and operated according to this control approach and will be discussed within this paper (Figure 13-11).

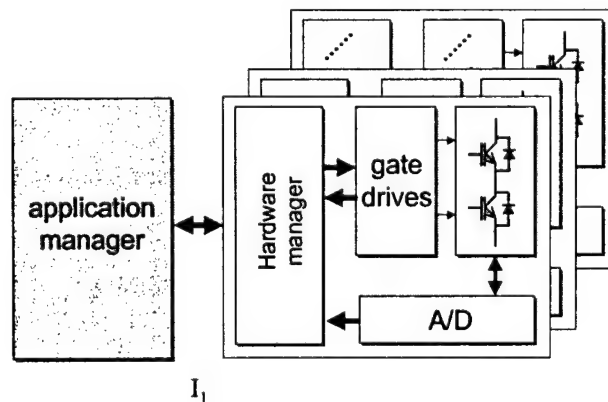


Figure 13-2. New system architecture.

13.2.1 Application Manager

The application manager, envisioned as a high level controller liberated from any kind of low-level hardware-oriented tasks, was designed to provide system flexibility and ease of software reconfiguration. It is specifically designed to perform higher-level control algorithms and supervisory tasks.

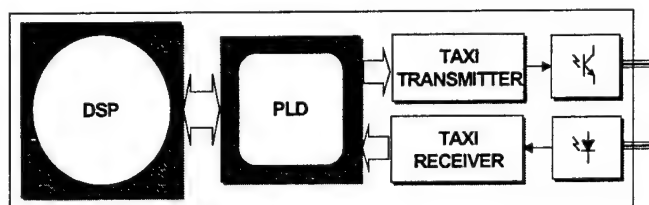


Figure 13-3. Block diagram of new, universal DSP controller.

As designed it consists of DSP, electrically programmable logical device (EPLD) and serial I/O port (shown in Figure 13-3), which provides open control architecture capable of controlling multiple independent PEBB modules. The structure of the controller is totally independent of the converter topology, number of switches, sensors, etc. The DSP, which serves as a powerful yet flexible tool is designated for accomplishing application-specific tasks, thus yielding a high level of system adaptability.

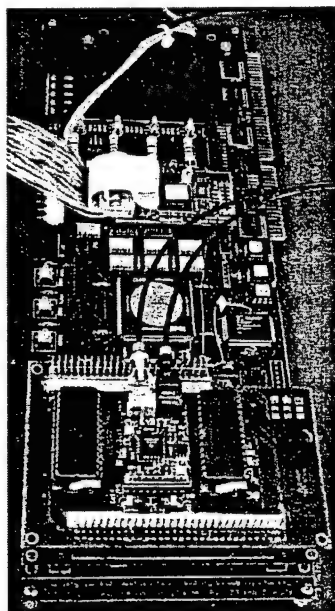


Figure 13-4. Universal DSP controller board.

System reconfiguration is achieved by simple software management. Providing an additional library of different programs for different control tasks would reduce development time and cost significantly, while reconfiguration of such a system then becomes solely a software-related issue.

13.2.2 Hardware Manager

The hardware manager, designed as an integral part of the PEBB module, is responsible for hardware-related tasks such as: PWM generation, low level module protection and communication and sensing of all key analog variables. The hardware manager is application-independent, and is envisioned as an encapsulation of the hardware designers' knowledge to control and protect the power circuit. The vision is inclusive of the building block approach, meaning that the hardware manager itself should lend itself to hierarchical implementation.

Depending on the power level and system requirements, the hardware manager can be designed for different power converter topologies or even sub-topologies. For example, the hardware manager can be designed for a single phase-leg or for a whole three-phase converter.

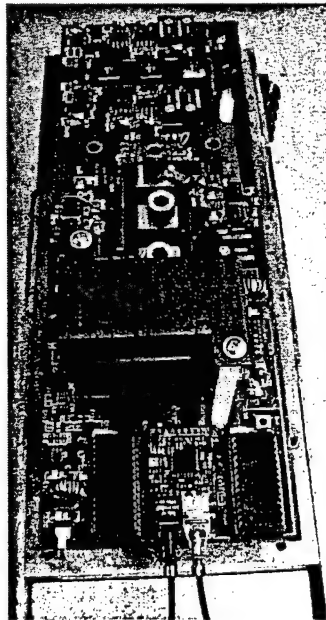


Figure 13-5. Integrated “smart” PEBB module based on ZCT phase-leg.

Once the communications interface is defined, this method of control partitioning allows the selection of the application controller (based upon the application requirements) and the hardware manager complexity based upon the topology and performance criteria. Both of which are programmable and reusable.

13.2.3 Communication Link

One of the gears that make the distributed controller system flexible, open, and modular is the communication protocol [8]. Our ultimate goal is to design a reliable, inexpensive, fast, and open control structure that would follow plug and play (PnP) principles. The more information we communicate the more flexible a system we get, but since the bandwidth of the communication channel is limited, a trade-off has to be established. The communication network that we proposed and designed, together with the protocol, is based on the high-speed (125 Mbits/sec) daisy-chained serial fiber optic link [8].

Two basic types of information are being communicated through the network: real-time data, exchanged on switching cycle level, and initialization data exchanged during the system power up. Data that is being communicated from the application manager to the hardware manager is desired phase leg duty cycle and switching period. Feedback data is provided from the hardware manager to the application manager in the form of current, voltage, temperature and status information.

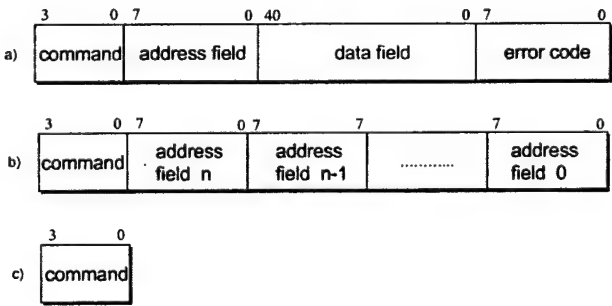


Figure 13-6. Data formats in distributed controller network.

- a). Data frame.
- b). Synchronization frame.
- c). Command frame.

The format of the data packets that are transmitted through the network is shown in Figure 13-6. The specific number of bytes always follows a command that allows a receiver to identify the type of incoming data.

13.3 Implementation of Single Phase-Leg PEBB Based Hardware manager

As previously explained, a single-phase leg has been identified as the basic building block that provides good tradeoff between flexibility (defined as the number of realizable topologies with the basic cell) and added control and communication complexity.

For two-level converters, using the components described earlier as basic building blocks, topologies such as the full bridge converter, the three-phase VSI, or the three-phase boost rectifier can easily be assembled. For some multi-level topologies such as the flying capacitor, this cell can also be identified as a universal building block cell, while for others, such as neutral point clamped (NPC) converters, small changes are needed.

13.3.1 Functional Description

The hardware manager or “smart” gate drive is designed to perform several functions (Figure 13-7) such as:

- PWM generation for main and auxiliary switches;
- Isolated gate-drive for both main and auxiliary switches;
- Over-current protection and indication;
- Current, voltage and temperature sensing and AD conversion; and
- Communication of PWM, status and measurement information.

The only information the power module communicates with is a standardized serial data packet going in and out of the module in a daisy-chain manner [8]. All the necessary data for proper module operation are encoded in the packet. Also, all the status information and sensed variables are sent back to the application manager, providing full control over converter operation.

If we impose a standard on the communicated data format, we can envision different manufacturer modules, connected into the same control network, controlled by a single application manager, forming single or multiple converters that can drive one or more loads without conflict.

13.3.2 Hardware Design

The hardware manager, shown in Fig. 5, as designed consists of gate drives, a high speed ALTERA 10K PLD, two AD converters, a high-speed ECL logic data transmitter and receiver, and a 125 Mbits/sec optical transceiver on a single board. Its main role is to assure proper operation of the phase leg module in a daisy-chained control network and to provide all necessary information to the application manager for performing closed loop operation of all converters connected in a network.

The communication interface, within hardware manager is built in three layers (according to ISO/OSI standard):

- The physical layer is provided by means of an inexpensive plastic optic fiber, while interface between data link layer and physical layer is achieved using HP optical transceiver.
- The data link layer is provided by a TAXIchip™'s [10] (transmitter and receiver), an optical signal coming in is fed to the TAXIchip™ receiver. The receiver converts the serial stream into parallel, which then goes to the EPLD.

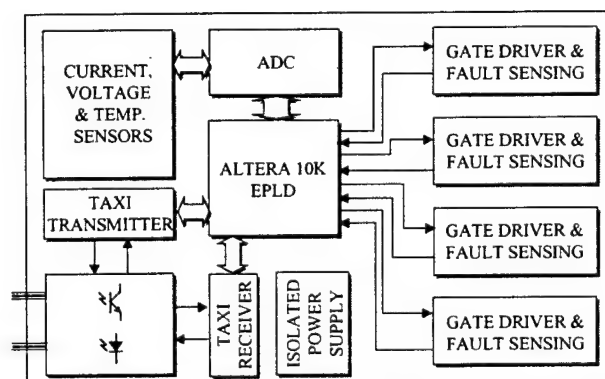


Figure 13-7. Block diagram of designed hardware manager.

Similarly, outgoing data from the PLD (in parallel form) is transformed by the TAXIchipTM transmitter into a serial stream, and then amplified by the optical transceiver [11] and transmitted through the optical fiber.

- The communication and control block, which is implemented in hardware (PLD), handles all network layer functions. A block diagram of the implemented functionality is shown in Fig. 6. The communication and control subsystem can be viewed as a small RISC processor receiving commands through the network and executing commands. Its basic modes are described as:
 1. idle mode (waiting for the data packet),
 2. forward mode: when it is just passing the information to the following node,
 3. active mode (incoming data packet has the address of the node): when the data is being first verified by CRC checker and then stored in corresponding buffers and the packet is then forwarded with the results of current/voltage/temperature measurements and local status information,
 4. synchronization mode (after receiving SYNC command from application manager): which reloads the double buffers, initiates AD conversion and resets PWM generator and
 5. initialization mode: which initializes the whole system and dynamically assigns the node address.

The PWM generator and local fault protection are also realized in the PLD. A functional block diagram is shown in Figure 13-9. Three main parameters necessary for proper operation of PWM generator are: duty cycle, switching period and the synchronization command. The duty cycle, when received and validated for proper transmission, is being stored in buffer 1. This information is becoming active only after a received synchronization command from the application manager, which moves the duty cycle information into buffer_2. Buffer_2 is active and is used for PWM generation. Period

information (which controls switching frequency of the leg) is also double-buffered for the sake of proper synchronization. A digital comparator compares the content of the counter with duty cycle information and creates a control pulse for the switch. The dead time generator and fault protection are the final stages in PWM generation, providing shoot-through and over-current/voltage/temperature protection.

Data acquisition subsystem is shown in Figure 13-10. Most of today's control systems in power electronics are based on full-state feedback, which requires per-switching cycle current and voltage measurement. Therefore, the designed hardware manager consists of current, voltage and temperature sensors. Measurement of module voltage and current is performed simultaneously per switching cycle using two 12-bits AD converters, while temperature measurement is performed at 10 times slower rate. Proper timing is achieved through a synchronization command received from application manager. Measurement results are stored in the output buffer, ready to be packed into a corresponding data packet. Onboard availability of these measurements allows for local current, voltage and temperature protection. All control functions and buffering are implemented within the EPLD.

13.4 EXPERIMENTAL RESULTS

One of the biggest concerns when mixed-signal boards are designed for power control application is EMI noise immunity. Since the hardware manager is an integral part of the power module the circuit board will be mounted in close proximity to the IGBT modules (Figure 13-12.), and will have to contend with high di/dt and dv/dt , due to the power device switching in excess of 20 kHz.

In order to verify the proper operation of the proposed system, the three-phase VSI was coupled with an RLC load. A block diagram of the VSI built from smart integrated phase-leg modules and controlled by the application manager through the high speed serial optical communication network is shown in Figure 13-11. An actual converter photo is shown in Figure 13-12. The three phase output voltage waveforms obtained from VSI operating in open loop are shown in Figure 13-13.

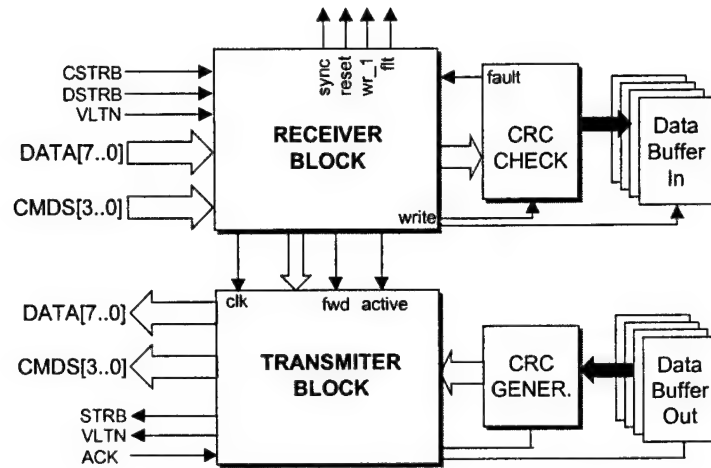


Figure 13-8. Functional block of hardware manager controller implemented in PLD.

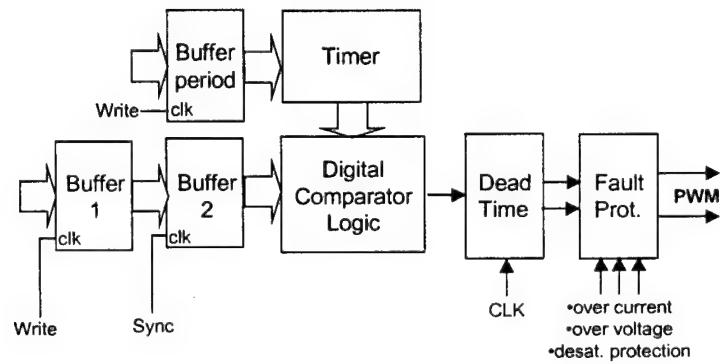


Figure 13-9. Block diagram of PWM controller.

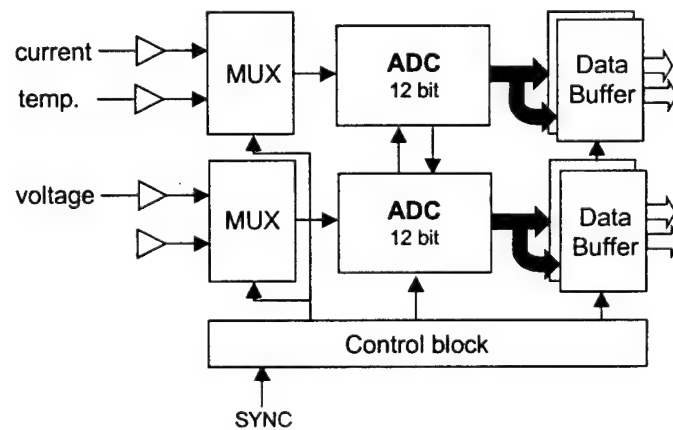


Figure 13-10. Block diagram of data-acquisition subsystem.

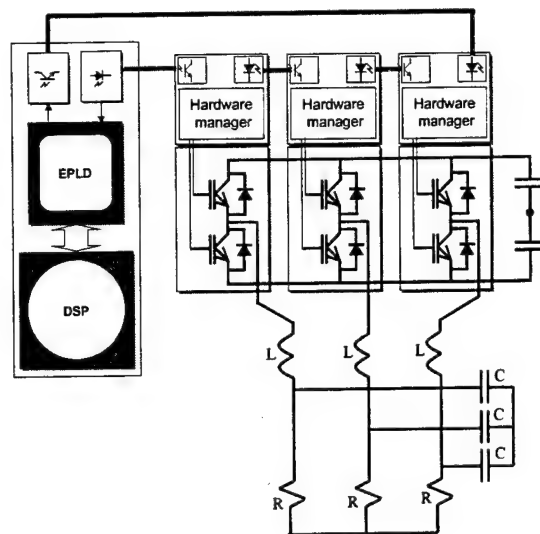


Figure 13-11. Block diagram of experimental setup.

($R=2.7\ \Omega$, $L=0.3\ \text{mH}$, $C=600\ \mu\text{F}$).

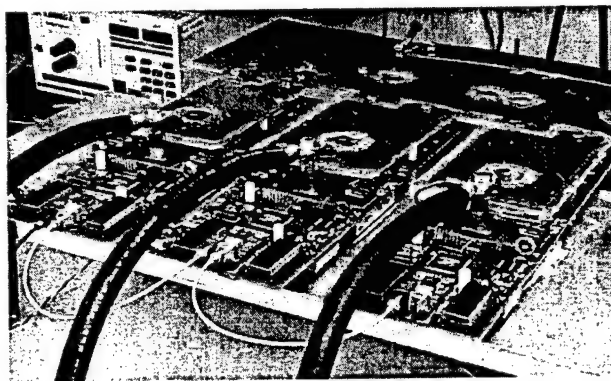


Figure 13-12. Three-phase VSI designed following distributed controller concept.

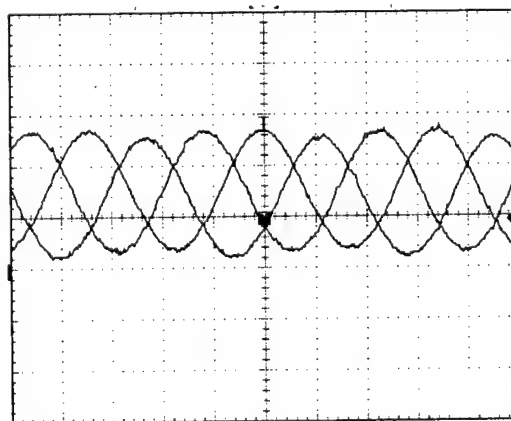


Figure 13-13. Test waveforms showing converter output phase voltages (50 V/div).

13.5 Power Electronics System Network - PES Net

PES Net is a control network tailored to the particular needs of power electronics systems. It is intended for use in power-converter systems for control data exchange between a power stage and a digital controller.

The task in designing this protocol was to come up with a smarter way to utilize the optical fiber link between the digital signal processor that controls the system and each of the phase legs or loads (nodes) of the converter system. This consequently would improve the reliability of the system, ease the hardware debugging process, standardize the interface and reduce the cost of building the system. Fewer fibers would be used and the number of transmitters, receivers, and engineers' time to implement control communication on such system would be brought down.

PES Net is, in fact, a more sophisticated way of using TDM. Information is sent using data packages, which have their destination address. Since asynchronous communication is implemented, the beginning of each packet is marked by pre-specified command.

A choice had to be made in respect to network topology. Because of the many benefits that the ring structure provides, and specifically because just the basic fiber-optic components are needed, the decision was made to implement this structure. It is very important to use a simple technology, which does not require extensive user training. It is much easier to deal just with optical fibers, transmitters and receivers, than also with splices and optical stars.

The control network design for converter module communication is based on a MACRO and FDDI protocol.

13.6 Protocol Functioning

In the communication sense, this is a ring structure, as shown in Figure 13-14. One fiber leaves each of the nodes, and one comes in. Information is sent in only one direction. For the sake of redundancy, a double ring can be implemented.

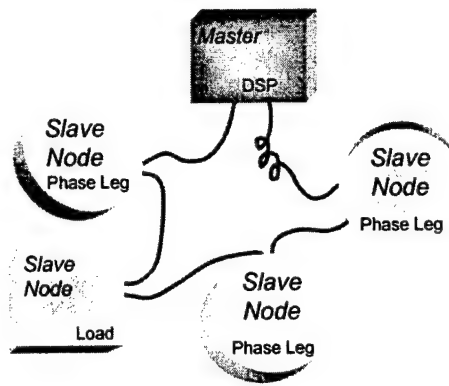


Figure 13-14. Ring nature of proposed topology.

This is a master-slave structure, in which the converter controller is a master and power modules are slaves. The master first transmits data packets for each of the slave nodes and then follows with a synchronization sequence. One communication cycle corresponds to one switching cycle of the converter.

In the passive state, slaves are just passing data to the next node. When the node recognizes its own address, instead of passing data to the next node, it starts sending its own data, while it stores the received data, as illustrated in Figure 13-15. When the packet is received fully and transmitted, node goes back to the passive state. Data measured on a power stage and status information are delivered to the controller.

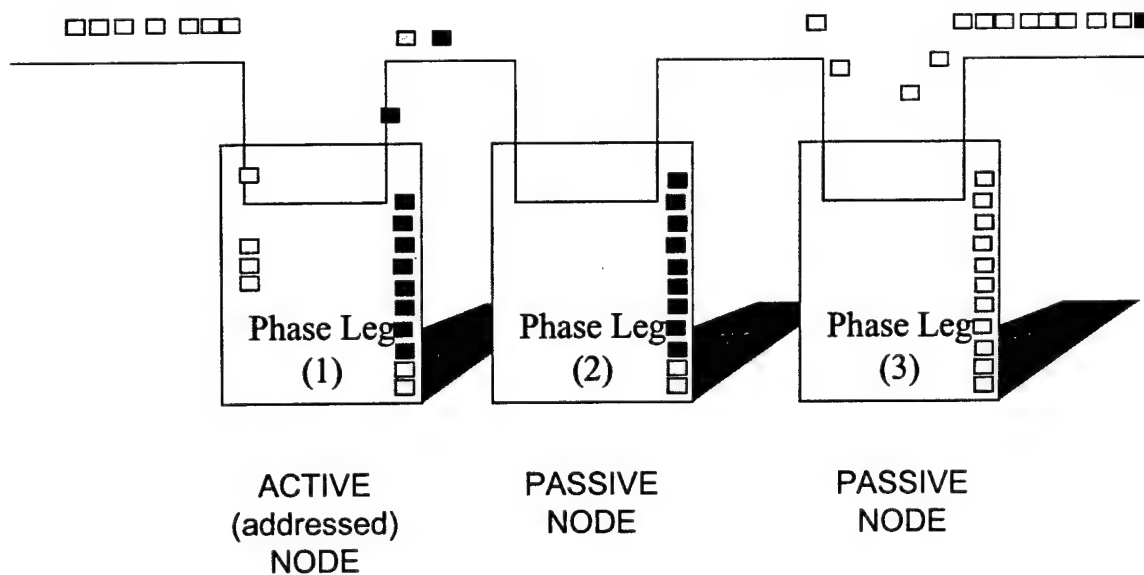


Figure 13-15 Ring Structure Functioning: Node (1) recognizes its address, transmits local data, and stores received data. Other nodes are just passing data down the line.

13.6.1 Protocol Layers

The PES Net protocol does not have all of the proposed ISO/OSI layers. The implemented layers are described below.

13.6.1.1 Physical Layer

In the designed system, the PL is plastic optical fiber link. Data that needs to be sent is transmitted in the light form over the link. The Hewlett Packard's HFBR-0507 series optical transmitter and receiver are used. The transmitter is a 650nm LED (HBR-1527). The receiver is a PIN receiver HFBR-2526. They allow data transmission of 125 Mb/s over 100 m. These components can be used with POF or HCS® fiber. Operational wavelength is 650 nm (red light). The fact that visible light is used is beneficial for debugging and safety purposes.

13.6.1.2 Data Link Control Layer

In the FDDI standard a four-bit data is coded into five-bit nibbles (4B/5B), making use of the most efficient combination for transmission with a NRZI scheme. In this scheme, ones are represented by transition, while on zeroes the signal remains the same. Use of NRZI coding makes clock extraction from the data stream possible. The used AMD's communication chip, TAXIchip™, receiver automatically does this.

The output of the optical receiver and input to the optical transmitter is a pseudo-ECL data sequence. Complementary pseudo-ECL signals are used. A transition between two levels represents logical one, while the lack of transition represents logical zero. This representation of the signal is particularly good for sending data over long distances or in noisy environments. A two-line complementary input/output of the fast signals is very appropriate for printed circuit board (PCB) routing, because it picks up less EMI noise.

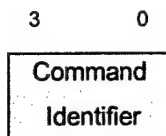
TAXIchip™ transmitter and receiver perform functions in this layer. Data is supplied to it on an 8 bit wide bus. TAXIchip™ adds two more bits to every 8-bit word, based on 4B/5B coding. This coding uses combinations of ones and zeroes, which are best for clock extraction and resynchronization on the receiver side. This coding is regulated in the FDDI standard.

13.6.2 Network Layer

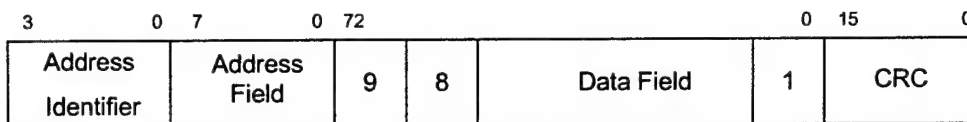
13.6.2.1 Data Formats

There are three types of data frames defined in the PES Net. They are: command frame, data frame and synchronization sequence frame, as shown in Figure 13-16.

Command Frame: Master-to-Slave



Data Frame: Master-to-Slave and Slave-to-Master



Synchronization Frame: Master-to-Slave

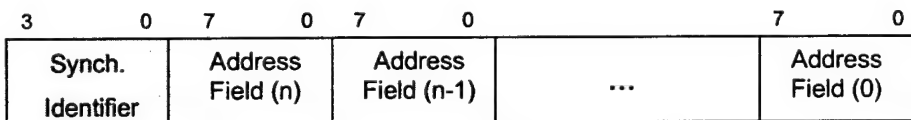


Figure 13-16. Data formats.

13.6.2.2 Data Frame

The data frame is 13 words long: nine bytes are for data, one for the address field, two are CRC and one word is the address identifier, as shown in Figure 13-16.

The address identifier command marks the beginning of the data frame. Following is the node address and data fields. The address field is eight-bits long, so theoretically up to 255 nodes can be supported. In MACRO protocol, the address field is divided in two. The first part determines the master address, while the second one determines the slave address. This allows the ring to have multiple masters. In the PES Net, the upper three

bits are reserved for possible multiple master addresses, while the lower five bits can address 32 slave nodes.

The frame sent by the master has eight bytes intended for real-time data (PWM information) and one for non-real-time data. The PWM signal information can be sent in two ways. The simplest way is to send two digital 8-bit values: the ‘up’ time, t_{up} , and the ‘down’ time, t_{dn} . Based on these two values, on-board digital logic can generate a PWM signal (Figure 5.4). Two time values are given and implemented in reference to the synchronization pulse. The controller sends these two values for every switch.

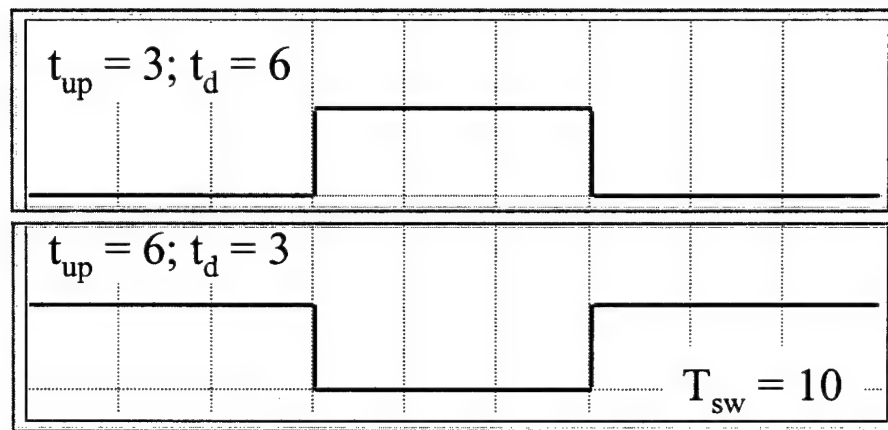


Figure 13-17. Generation of PWM signal based on two-byte digital information.

Table 13-1 Adopted data field format in master-to-slave data frame

Data Byte	Purpose
Data 9	Non-real time
Data 8	t_{down} for the switch n, higher byte
Data 7	t_{down} for the switch n, lower byte
Data 6	t_{up} for the switch n, higher byte
Data 5	t_{up} for the switch n, lower byte
Data 4	t_{down} for the switch p, higher byte
Data 3	t_{down} for the switch p, lower byte
Data 2	t_{up} for the switch p, higher byte
Data 1	t_{up} for the switch p, lower byte

In the soft-switching case, the PWM signals can be locally generated. This is possible because there is some form of local intelligence on the PEBB board and because the PWM signals for the auxiliary switches are related to the PWM signals of the main switches. The shape of the auxiliary PWM sequence depends on the used soft-switching

technique, but both PWM signals can be generated based on the t_{up} and t_d for the main switch. Consequently, the auxiliary PWM signals are generated on the slave board, without sending any extra information. Parameters necessary for the auxiliary switch PWM generation can be negotiated in the initializing phase. The other option is to allocate a space in a data frame for auxiliary switches t_{up} and t_d , and treat them, in communication terms, in the same way as the main switch transition times. Any other combination of different timing instants with different resolutions can be implemented, as long as the total information can be coded with 64 bits in every switching cycle.

Table 13-2 Adopted Data Field Format in Slave-to-Master Data Frame

Data Byte	Purpose
Data 9	Status
Data 8	Non-real time data
Data 7	Non-real time data
Data 6	Real-time data, higher byte
Data 5	Real-time data, lower byte
Data 4	Voltage, higher byte
Data 3	Voltage, lower byte
Data 2	Current, higher byte
Data 1	Current, lower byte

The frame sent by a slave node has six bytes intended for real-time information (digitized current and voltage values) and three for non-real-time data (temperature, fault and status information). The data formats adopted in this thesis are given in Table 13-1 and Table 13-2.

13.6.2.3 Synchronization Frame

The algorithm implemented is a synchronization sequence described in Chapter 4. The master sends a synchronization sequence when synchronization is required. Each slave node recognizes the 'Sync' command and goes into the synchronization-state, within which it waits for its own address. When the address is received, it generates a synchronization signal for its phase-leg.

Synch. Identifier	Address n	Filler	Address (n-1)	...	Address 1
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Figure 13-18. Synchronization Frame.

The format of this sequence is shown in Figure 13-18. Synchronization Frame. The frame starts with the synchronization identifier, and is followed by the several 8-bit-long data blocks containing addresses of slave nodes and filler fields. The first address to be transmitted is of the slave node that is last to receive the frame. The number of address data blocks sent equals the number of slave nodes on the ring, which we want to synchronize.

The ‘filler’ is used to implement the delay into synchronization frames. From the hardware and software implementation point, the simplest way to define the filler is in terms of data words. Instead of having an extra timer that would measure the desired delay, it is much simpler to send several empty data bytes in between the address fields of a synchronization sequence.

For example, in the implemented three-phase system, the measured propagation delay through one node is 468 ns. This delay is approximately equal to four or five data words, because it takes 100 ns to transmit one word at ring speed of 125 Mb/s. If four bytes are used, the synchronization sequence is shorter, so the bandwidth of the whole system is affected less. In the case that a five-word delay is used, synchronization is more precise.

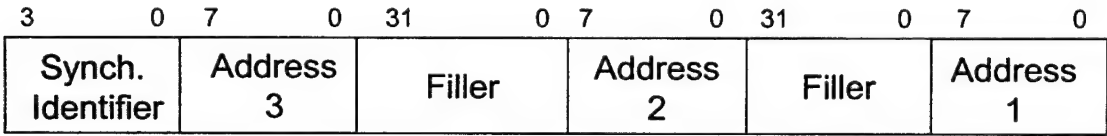


Figure 13-19. Synchronization frame for the three-phase converter.

The synchronization sequence for a three-phase system (one master and 3 slave nodes), shown in Figure 13-19, is formatted as follows:

- A synchronization identifier is followed by the address of the node that is the last one to receive the frame (node 3 in Figure 13-18),
- After a 5-byte delay (the node address and 4 empty data words, which takes 500 ns to transmit), it sends the address of node 2.
- After another 5-byte delay, it sends the address of node 1.

Use of this algorithm reduces the propagation delay from 468 ns to $(500 \text{ ns} - 468 \text{ ns} =)32 \text{ ns}$. This means that its implementation delay is reduced by 93%. If needed, an even better synchronization can be achieved, but a more complicated implementation is required. For that purpose, a delay would be defined in terms of master node's clock frequency or as fraction of data words.

This algorithm relies on a specific ring topology. The delays are independent of the switching frequency of the converter, but are related closely to the data transmission rate. An increase in communication speed causes a decrease of propagation delay.

There is one more assumption made, and it concerns the state of a TAXIchip: the slave node has completed sending the last package-byte to-be-transmitted. This should always be true because the slave speaks only when spoken to, and transmits the same number of bytes that it has received. Otherwise, a TAXIchip may have a buffered byte of data that is waiting to be sent, which would distort the timing of a synchronization sequence.

It is a good practice to induce a taxi-synchronization command to be sent prior to the ring-synchronization sequence. This forces the TAXI-receiver to re-synchronize its clock to the TAXI-transmitter clock. Because of this, the time between the last byte transmitted and the beginning of the synchronization sequence should be about 1.5 of the line-word length (duration of 15 line-bits or 120 ns), but, if possible, it could wait the time for the full length of the package to be transmitted.

Slave nodes use the synchronization pulse generated during the synchronization sequence as a time-marker for resynchronization of the digital counter logic, which controls A/D converters and PWM generator. Use of A/D with a built-in multiplexer allows a use of the same A/D for the conversion of current, voltage and temperature. The most critical and fastest changing variable, such as current, should be measured last and as close as possible to the time when data is sent to the controller. The least critical and slowest variable, such as temperature, should be measured first.

13.6.2.4 Command Frame

Command frames consist of one word - the actual command, as shown in Figure 13-16. Since TAXIchip™ is coding 8-bit data word as a 10 bit word (because of 4B/5B coding) not all of the combinations are utilized for data word coding. The unused combinations are defined as commands. TAXIchip™ receiver has a separate output bus for data and separate for commands.

A total of 15 different commands can be specified. Six are predefined.

- Address Identifier: Marks the beginning of the data frame.
- Network Synchronization Identifier: Marks the beginning of the synchronization frame.
- Shutdown Identifier: Sent by the master when shutdown of the system is desired.
- Mater-Reset Identifier: Sent by the master when reset of the system is desired.
- TAXI Sync Command: Used to keep TAXI-Rx synchronized to TAXI-TX. This is generated automatically by TAXI-TX.
- Broken-line Indicator: No light in the incoming fiber.

In the case of a broken line (no light in an incoming fiber), TAXIchip will detect this as a reception of a ten zero bits. This is interpreted as a command “1111 1111”. This command is not used in this protocol, so reception of such a command indicates the broken line or improper function of TAXIchip™ transmitter. In the case when there is no data to send, the TAXI-TX would send a TAXI synchronization command, and it would never allow TAXI-Rx to receive the stream of ten-bit zeroes, since it can be interpreted as a valid command. This particular command can be used for the detection of a line failure. This sequence is not used for any other purpose by the protocol, so the node knows that failure has occurred in the case of a repetitive reception. After a failure is detected, the block can employ a converter shutdown.

13.7 Conclusion

We have presented a new approach for the control of medium and high-power converters. The new distributed controller architecture as proposed and implemented provides several prominent features:

- Hardware independent, universal controller capable of controlling multiple converters;
- Open and flexible communication protocol for distributed control of smart PEBBs;
- Flexible, transparent and easy to use power modules
- Simple system integration and reconfiguration.

The hardware design for the proposed controller is based upon the off-the-shelf components widely used in other engineering areas (especially in computers and communications), which brings us to conclude that the overall controller cost will be significantly reduced, regardless of the future smart module market.

We believe that further optimization, and integration of the power stage with the hardware manager (using some of the advanced packaging techniques) will lead to a wide spectrum of reliable, compact, flexible and easy-to-use power processing units that will inevitably change power electronics design and practice. Additionally, as a result of the control partitioning, standard application control libraries can be established. Taken together, standard power modules, and software libraries would result in reduced non-recurring engineering cost, faster time to market and the economy of scale for medium and high power electronic applications.

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